

IC Validator

Overview

IC Validator is a signoff DRC/LVS tool that has been architected and proven for in-design physical verification at leading-edge process nodes. It delivers excellent scalability for efficient utilization of available hardware, superior ease-of-use for the physical designer, and high programmability for easier sunset development.

IC Validator's high performance DRC and LVS physical verification engine substantially reduces the time to results through near-linear scalability across multiple CPU cores.

IC Validator is seamlessly integrated with IC Compiler for In-Design physical verification. This award-winning technology accelerates design closure for manufacturing by enabling independent signoff quality analysis and automatic repair, including Double Patterning Technology (DPT) decomposition checking — all within the implementation environment.

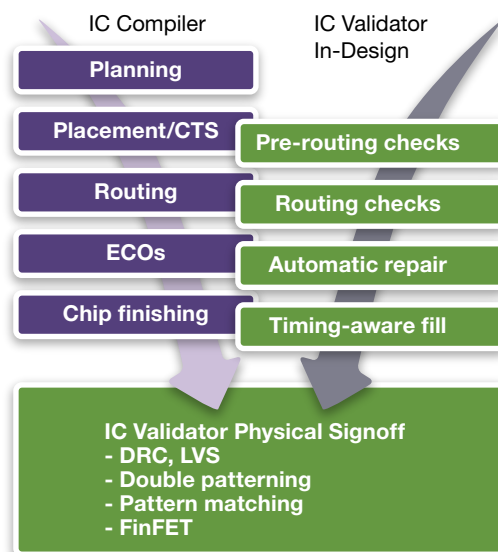
IC Validator is fully qualified and silicon proven by major foundries and IDMs for physical signoff at advanced nodes.

Benefits

Turnaround Time

Prevailing approaches to physical design today can be described as implement-then-verify, resulting in multiple time-consuming iterations between design and signoff. This cumbersome flow is due to the lack of signoff-quality physical verification during design implementation. At the 40nm technology node and beyond, the implement-then-verify flow is slow and may complicate convergence as layout corrections can alter key design metrics such as area, timing and power. And, at 20nm, the introduction of a clear new challenge, DPT compliance, is placing an unprecedented burden on physical designers.

IC Validator is specifically architected for in-design physical verification, bringing the power of full signoff physical verification constraints into the design phase without imposing time-consuming stream-in and stream-out of layout data. Using in-design physical verification, DRC and manufacturing issues are caught much earlier in the design cycle, reducing or eliminating late-stage surprises close to tapeout. With in-design verification, specific layer, rules and selected areas of layout can be targeted incrementally, providing a speed-up in overall design completion time. Design rule violations discovered during verification — including DPT limiting layout



IC Validator physical verification solution

patterns — can be automatically fixed within the global timing and area context of the design, reducing the impact of the correction. In addition, chip finishing operations typically performed during physical verification, such as metal fill, are managed in a similar fashion. Working with IC Compiler, IC Validator's in-design flow delivers significantly faster runtimes and dramatically reduces chip finishing iterations by performing signoff quality, timing-driven metal fill and also double patterning decomposition during the design phase.

High Performance and Scalability

The complexity of the physical verification task has grown substantially at the 40nm process node, and is getting worse at 28nm and beyond. To address the capacity and performance requirements of physical verification at advanced nodes, IC Validator is architected for excellent scalability and efficient utilization of available hardware.

Multithreading: IC Validator's multithreading approach significantly shortens execution time on modern multicore CPUs.

Scalability: IC Validator provides near-linear scalability across a distributed computing network, supporting a 24X run time acceleration on a 32-CPU network and enabling completion of any physical verification task overnight (See Figure 1).

On-Demand Load Balancing: Intelligent job scheduling keeps all cores equally busy to minimize the total job completion time.

Memory-Aware Scheduling: IC Validator's scheduler distributes jobs so as to avoid exceeding any individual computer's memory capacity. This avoids delays caused by paging when memory is exceeded.

Performance scalability

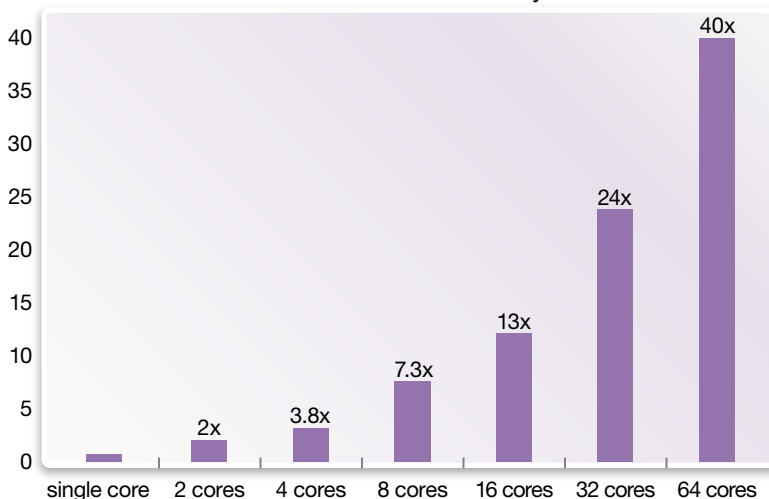


Figure 1: IC Validator scalability extends to 32 cores and beyond

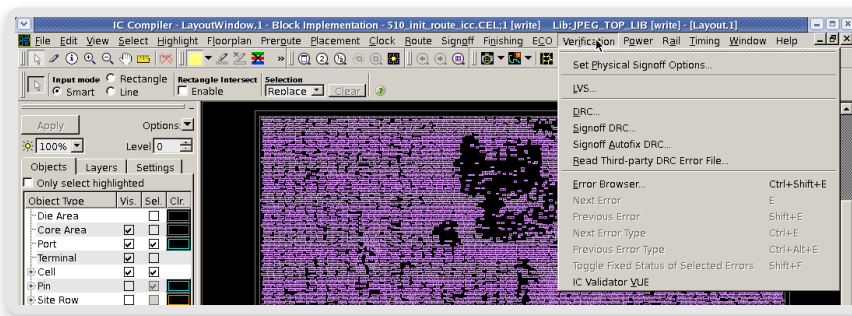


Figure 2: IC Compiler GUI showing IC Validator-enabled signoff DRC commands

Enhanced Productivity with In-Design Physical Verification

Automatic DRC Repair (ADR)

IC Validator's seamless integration with IC Compiler enables an innovative layout auto-correction interface, which identifies DRC violations — including DPT decomposition violations — and initiates automatic repairs. The corrections are applied by IC Compiler to alleviate DRC and DPT errors, and then validated within IC Validator. In-Design integration makes it possible to maintain hotspot-free designs throughout implementation, further eliminating iterations with downstream analysis tools. ADR's tight find-and-repair loop enables rapid discovery and

repair of errors, minimizing designer intervention and speeding time to tapeout. (See Figure 2).

Incremental Layer-based, Rule-based and Area-based Verification

To accelerate physical verification time, IC Validator and IC Compiler integration enables intelligent incremental flows to eliminate unnecessary checking by restricting verification to the specific layer, rule or design area that needs validation. The tight integration provides a powerful tool dialog that allows the user to quickly select the rules, layers and region size for DRC checking, pattern matching, or adding metal fill. By automatically limiting the scope of the validation, more verification runs

can be performed early in the design cycle, greatly reducing the number of full design verification runs, and shortening the time to results. (See Figure 3)

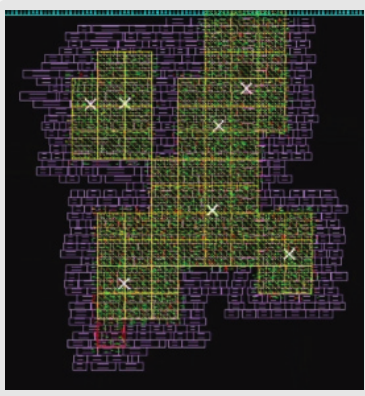


Figure 3: Area-based incremental signoff DRC analysis. Only the highlighted area is submitted for analysis

Incremental verification is especially important for ECO validation, which typically impacts a very small section of the design. Using a conventional flow, critical verification time can be wasted on checking the full chip even when changes were made to selected regions or layers. The In-Design flow saves time by restricting the verification to only the layers and area affected by the ECO. As a result, the In-Design flow significantly speeds verification without undue burden on the physical designer.

Timing-Aware Fill

At advanced nodes, fill insertion is mandatory to ensure manufacturability and high yield. But excessive fill can lead to build up of coupling capacitance, impacting timing and resulting in unpredictable iterations with design. In-Design technology with IC Compiler and IC Validator enables single-pass fill implementation that is timing aware to prevent such problems. Combined with IC Validator's novel fill-to-target technology, timing-aware fill efficiently balances timing and density and replaces multiple fill-analyze iterations with a single step.

Error Visualization

To maintain efficient physical verification, rapid visualization and error correction are as important as fast physical verification runtime. IC Validator includes the IC Validator VUE visualization tool, which provides an easy-to-use, intelligent error navigation and prioritization system for efficient review and correction of DRC and LVS issues, double patterning conflicts, and manufacturing-limiting patterns. Using IC Validator VUE, layout engineers can quickly and easily scan physical verification errors in IC Compiler environment, as well as other widely used layout editors. IC Validator VUE enhances productivity for physical verification engineers.

Pattern Matching

IC Validator's Pattern Matching efficiently expands IC Validator's rule-based signoff engine for pattern-driven verification. This capability makes it possible to very quickly identify and automatically correct manufacturability hotspots in a design, by comparing against a library of known problematic layout patterns. IC Validator's patented pattern matching technology eliminates the need for convoluted rules and, with almost zero runtime penalty per pattern, it significantly speeds up the time to achieve manufacturing compliance.

Signoff Ready at 28nm and 20nm

Foundry Qualification

Comprehensive foundry qualification is a necessary component of any successful physical verification solution. IC Validator is designed specifically for 45nm and smaller nodes, and is qualified and actively in use for finFETs, SOI and traditional technologies at 45/40nm, 32/28nm, and 20nm nodes by leading foundries.

Layout-vs.-Schematic (LVS)

IC Validator LVS is qualified at leading foundries and provides a comprehensive verification and debugging environment. The most important aspect of any LVS is the power and efficiency of its debug environment. IC Validator excels with its VUE and Shortfinder tools that quickly and easily identify errors, such as text-level shorts, for rapid repair and revalidation. VUE is a graphical environment to display and cross-probe between layout and schematics, together with a sophisticated error management system. IC Validator LVS device extraction supports leading-edge technologies where device parameters are often affected by their proximity to neighboring devices through layout dependent effects (LDE).

Fill-to-Target Technology

IC Validator's Fill-to-Target (FTT) technology is a tile-based parametric fill engine that inserts the right shapes in the right places to give superior planarity and smooth fill density, even around macros. This correct-by-construction approach improves yield and speeds turnaround time by replacing the traditional iterative fill-analyze flow with a single-pass.

Double Patterning

Manufacturing at 20nm and below usually relies on DPT, which requires that a design be decomposable into two overlapping layout patterns. IC Validator offers comprehensive support for double patterning developed in close cooperation with leading foundries and IDMs. IC Validator includes a native coloring (decomposition) engine based on flexible coding of DPT rules, and supports advanced capabilities such as stitching rules. With In-Design technology, IC Validator provides not only signoff quality decomposition checking, but also automatic repair of DPT conflicts. (See Figure 4)

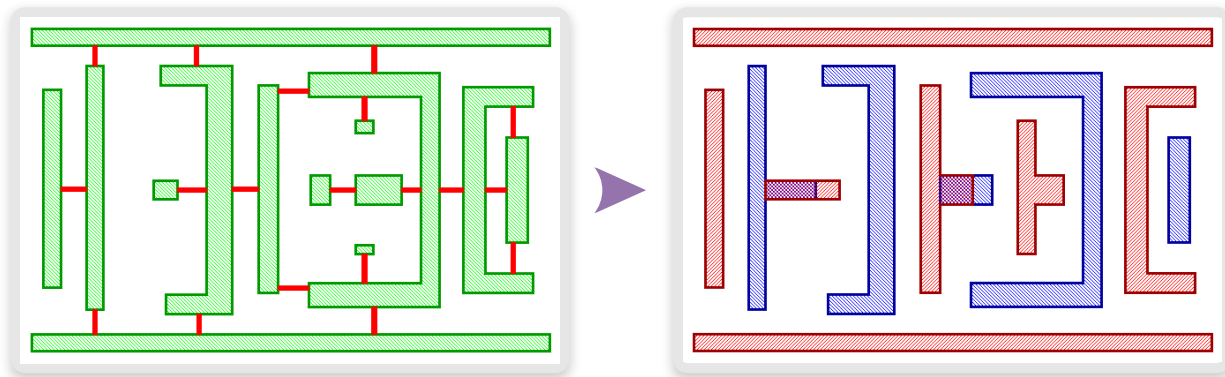


Figure 4: Signoff quality double patterning verification and correction is critical for 20nm and below

Equation-Based and Property-Based Checking

New foundry rules, like voltage-domain checks, often rely on specific properties that are attached to geometric shapes. IC Validator provides a flexible and efficient property-based checking mechanism to enrich physical verification beyond strictly checking geometries.

Other complex foundry rules can require localized and selective polygon inclusion criteria, or require continuous functions to describe accurately. IC Validator offers rich programmability features that can accurately compute equation-based geometric characteristics. For example, traditional binning can be too crude for critical area calculation, and a continuous equation-based evaluation is more accurate.

Flexible Error Reporting and Classification

IC Validator supports a DRC disposition and reporting utility that can implement custom DRC waivers and rapid categorization of DRC violations. DRC errors can also be reviewed as the DRC job continues to run. This approach speeds time to tapeout by enabling parallel debug and execution.

Integration with StarRC

IC Validator LVS has an efficient working flow with Synopsys StarRC™ for parasitic extraction. IC Validator supports end-to-end hierarchical parasitic extraction that minimizes physical flattening and simplifies extraction by implementing a single pass flow, providing a major performance increase over the double extraction flow of previous generation tools.

Integration with Galaxy Custom Designer®

IC Validator works together with Synopsys' layout editing tool, Custom Designer LE, to support a tightly integrated DRC and LVS-enabled custom design flow. Both IC Validator and Custom Designer fully support the OpenAccess database. In addition, Custom Designer is integrated with the VUE error navigator for rapid debug of DRC and LVS issues.

Interfaces and Platforms

Input and Output Data Formats:

- ▶ Milkyway
- ▶ GDSII
- ▶ Oasis
- ▶ OpenAccess

Supported Platforms:

- ▶ Linux32 4.0
- ▶ Suse 32
- ▶ Suse 64
- ▶ AMD64
- ▶ Solaris64
- ▶ Solaris64 x86_64
- ▶ Solaris32 x86_32
- ▶ AIX64

For more information visit:

www.synopsys.com/Tools/Implementation/PhysicalVerification