

When Following the Rules Is Not Quite Sufficient: The Need for New Post Route Analysis Techniques

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Problem Statement

Smaller technologies, shorter time to market windows and more complex designs are driving the need for an additional set of analysis techniques which will help designers understand how susceptible their designs are to manufacturing process variations. Technology nodes larger than 90 nm were able to achieve a certain level of manufacturability by complying with a set of foundry design rules. The high performance 130 nm and 90 nm nodes started to create the need for 'recommended' rules. These rules had slightly more stringent values for designs to meet and would, theoretically improve the manufacturability of those specific layout features. Another way to look at it would be: compliance to these values enabled designs to be less sensitive to manufacturing process variations.

It should come as no surprise that design teams became very concerned with understanding the manufacturability of their design. The terms design for manufacturing (DFM) and design for yield (DFY) have become common points of discussion as a result of this concern. With the popularity of customer owned technology (COT) design flows moving to advanced nodes like 65 nm, the need to maintain an acceptable level of manufacturability has not changed, just the complexity of maintaining it.

Any new method to understand design manufacturability used by design teams, mask manufacturers and semiconductor manufacturers requires predictability, fast time to results and accuracy. Achieving these three items ensures a smooth hand off to and from the design team every step of the way. With the adoption of 65 nm, it is clear that design teams require new analysis capabilities to reduce manufacturing surprises.

Components of Post Route Analysis

Yield is one common term used to understand a design's manufacturability. Traditionally yield is thought of as an artifact measured after a wafer was manufactured. Product engineers dealing with finished silicon were the primary recipients of any yield issues. The original design team was generally unconcerned with yield.

Today, design teams want to know how they can affect the yield of their designs. The cost of mask creation, wafers and schedule time require an additional level of manufacturing 'awareness.' Any analysis technique used by a design team to identify areas of potential issues requires access to accurate manufacturing information, the ability to perform accurate analysis using this information, and an efficient method for using this analysis to drive design implementation are requirements.

While every design team would like to know how their design will yield for any specific foundry process, this is an incredibly impractical and complex thing to achieve. It is more realistic to expect that design teams can improve their design's insensitivity to manufacturing process variations as opposed to actually calculating an actual yield number. While the phrase 'insensitivity to manufacturing process variations' is hardly a convenient acronym like DFM, it is reasonable to expect that certain portions of the manufacturing process can be understood well enough that design teams can provide a significant effect on how robust their design can be under those specific conditions.

Lithography Compliance Checking

Every technology node has added a level of complexity to the 'original' post route analysis technique – design rule checking (DRC). Design rules are no longer single values being applied to single layers to verify manufacturing compliancy. Today, a 90 nm process will include design rules that are a function of connectivity, multiple layers, and even device types. The manufacturing requirements for 65 nm have become so complicated that rules are no longer sufficient to ensure the optimum printability of desired shapes. At 65 nm and below, the number of rules becomes a daunting task to create and manage. Clearly, there is a need for a new yield analysis technique.

Lithography compliance checking (LCC) is a natural progression of the traditional design rule. It involves passing the knowledge of the actual lithography process in the design space. Traditionally lithography awareness was limited to the technologists focused on mask synthesis inside a foundry environment. Porting information about this process outside of this environment was considered not just unnecessary, but highly undesirable.

LCC poses unique challenges. The first challenge is balancing accuracy and performance. It is impractical to expect an entire lithography process to be performed on a full chip before it is passed to the foundry.

Critical Area Analysis

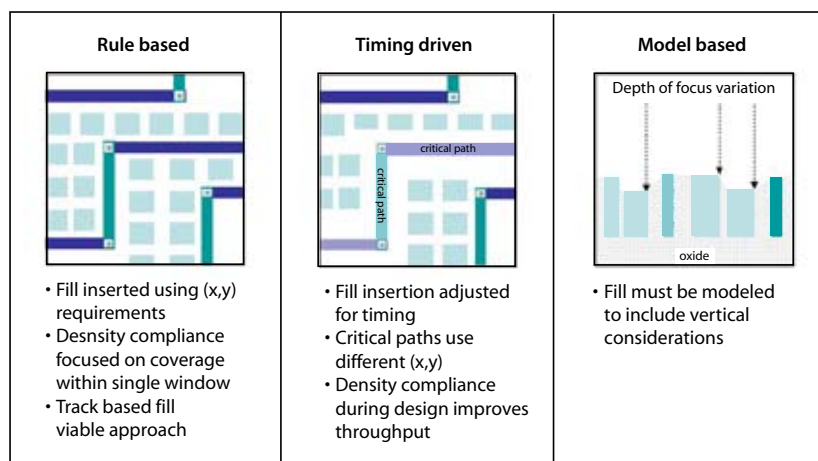
Critical area analysis (CAA) is the ability to quantify how susceptible a design is to random particle defects. These particle defects can cause unwanted shorts and opens between similar interconnect layers and between dissimilar interconnect layers. Information about particle size and the probability distribution of those particles can be used to create a heat map where adjustments can be made to reduce the effect of these random particle defects.

Model Based Dummy Fill

The insertion of dummy fill as a post processing step stepped into mainstream design with the 180 nm node. Maintaining design planarity enables good functional and parametric yield. Chemical mechanical polishing (CMP) was introduced to maintain planarity during the manufacturing process. It literally removes uneven surfaces after each new layer is added to a wafer by mechanically polishing the surface flat. Non-planarity causes variation in the depth of focus during lithography. Poorly printed images can result in functional degradation and even failure. Non-planarity also creates interconnect variation, which effects parametric yield.

Similar to DRC on technologies at 180 nm and larger, dummy fill was rule based. Adding fill as a function of two dimensional rules created sufficient fill density to ensure design planarity during manufacturing. As technology nodes shrank and new materials like copper were introduced, inserting and understanding the effects of dummy fill became more complex.

As with design rules, smaller technology nodes make it clear that following the two-dimensional rules is not enough. The 65 nm node is driving the need to actually simulate the CMP process plus any resulting layer thickness variations. Why? Inserting fill as a function of rules, enables fill to be managed in two dimensions. Variations in height are unaccounted for in a rule based approach. At 65 nm, the depth of focus becomes a significant effect in printability. Therefore, designers need to understand these three dimensional variations caused by CMP to intelligently insert dummy fill during layout



Evolution of Dummy Fill

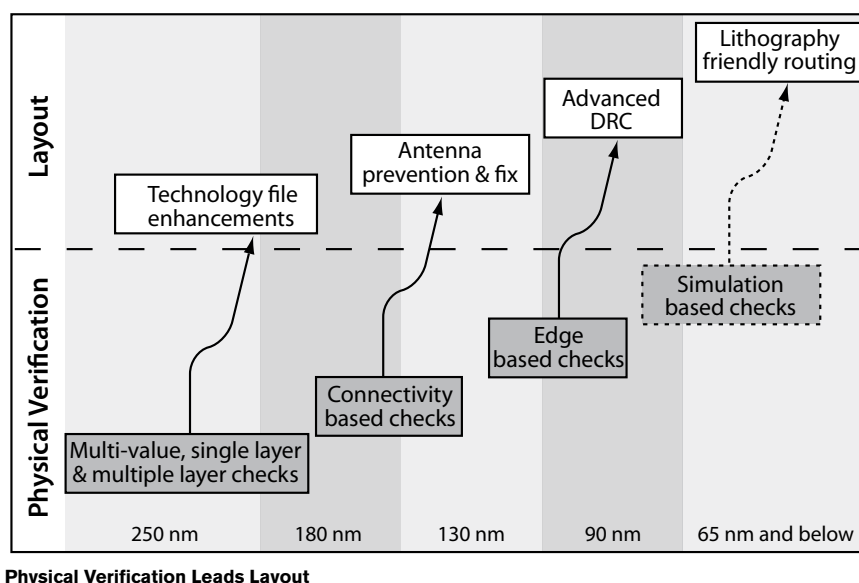
Giving Designers More Influence

There are two areas where designers can influence the manufacturability of their design. The traditional location is during physical verification. Physical verification has traditionally encompassed design rule checking (DRC) and layout versus schematic (LVS). A tape out or layout engineer will identify areas that are non-compliant and identify areas for the design team to fix. If a design is not DRC or LVS compliant, then it cannot be manufactured.

The downside of this flow is that valuable time can be lost fixing the violations identified at sign-off while trying to ensure desired design performance. Despite this single challenge, it is imperative that physical verification always be performed before passing a design to a foundry DRC and LVS provide the highest level of accuracy to design teams to verify manufacturing compliance.

The second area where designers can affect design manufacturability is during layout, before physical verification. Identifying and correcting these issues during layout does more than save valuable time. The effect of any changes can be thoroughly analyzed to ensure that design functionality is not compromised.

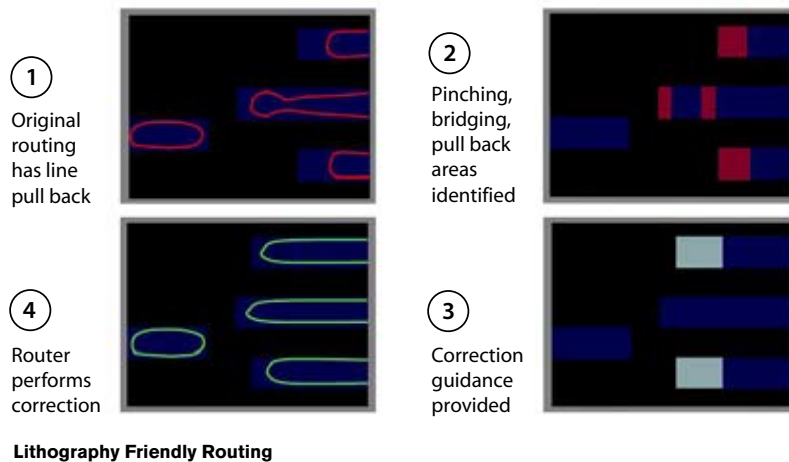
In the area of layout, physical verification rules have consistently found their way into the layout. The diagram below highlights which rules have migrated per technology node. The key observation to make is that regardless of the complexity, a few things remain constant. First, any new rule being added to the layout environment needs to have correlation to physical verification, and ultimately silicon. Second, the demand for results at each stage, layout or physical verification, remains the same regardless of the increase in complexity and data volume



Every technology node has expanded the amount of physical verification information being pushed into layout. The latest example of this is in the area of lithography friendly routing. Designs using 65 nm and below are highly susceptible to systematic yield loss caused by lithography effects. While rule based DRC is continues to ensure a baseline level of manufacturability, it is clear that rules are not enough. A design can pass DRC and have situations where it cannot perfectly print due to lithography challenges.

Clearly, there is a need to explore new physical verification techniques. Today, simulation based checks are emerging as a potential new sign-off supplementary method to verify a design's ability to be lithography compliant. Similar to the traditional rule based DRC, it is expected that this new approach will require silicon correction for accuracy, and a path into layout to maximize design team productivity.

Lithography friendly routing uses information from lithography simulation results to do two things. Firstly, the routing engine will minimize potential lithography issues using a known framework of rules and known lithography 'friendly' patterns. Secondly, the routing engine will work closely with a simulation based verification solution that will detect actual lithography issues and then provide correction guidelines to the router.



Foundry Partnerships Expand

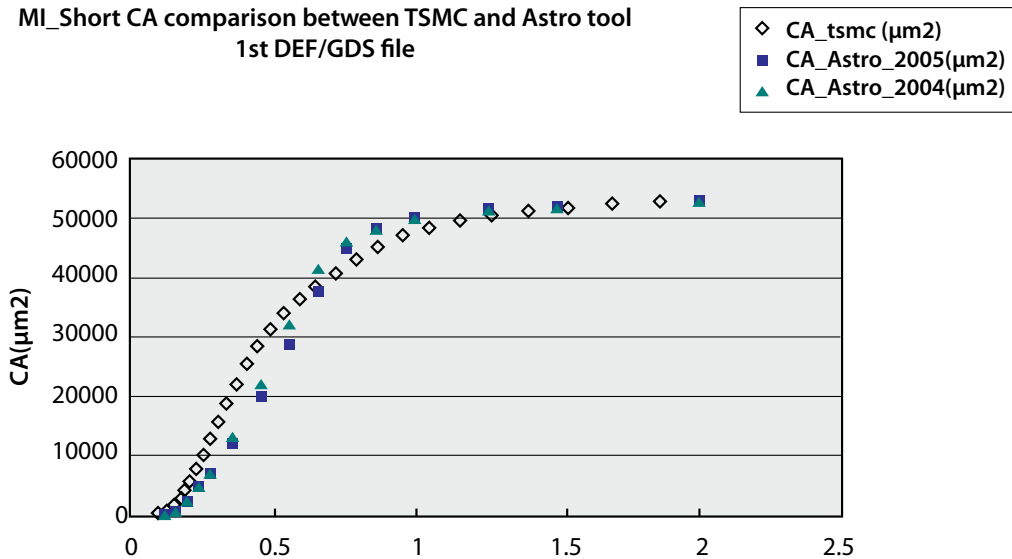
The fundamental criterion for any analysis solution is accuracy. One degree of accuracy is how well a solution can identify and measure a specifically identified situation. Any viable yield analysis solution will deliver this level of accuracy.

Another degree of accuracy is how well real process data is reflected inside the yield analysis technique used. A foundry partner is required to provide such information. Foundries have always provided some level of process information in the form of rules, but as this discussion has proved, rules are no longer enough. Additional information such as process defect distribution, lithography modeling, and dummy fill emulation are all new types of information required to achieve results correlated to silicon the best.

There is a tight balance needed between foundries and yield analysis tool providers to protect process IP and to ensure mutual customer success. Encryption technology, joint development partnerships, and exhaustive correlation exercises create a new level of co-development. Every participant provides their level of expertise – process knowledge, lithography modeling, and design implementation. The result is a well correlated flow of information from silicon to design.

One example is in critical area analysis. Critical area analysis can be performed as a post-route yield calculation using process data on actual measured defect counts. This can be correlated to a statistical method applied to a wire spreading algorithm embedded in a place and route solution. The figure below displays three sets of data. The blue points are actual critical area calculations using process data. The green and pink points are critical area calculations used by a place and route environment, based off of a statistical approach. Both approaches track each other well.

MI_Short CA comparison between TSMC and Astro tool
1st DEF/GDS file



The data shown above is one example of ensuring that the information used for analysis during implementation is correlated to the results generated with a post-route yield analysis solution and a foundry's process data.

Conclusion

For 65nm and below, following the rules may not be enough. Traditional rule based yield analysis solutions are not sufficient to ensure acceptable higher yield at 65 nm and below Applications such as lithography compliance, model based fill, and critical area analysis are indications of the increased desire for design teams to understand and influence design manufacturability. Maintaining a well correlated link from process data into design implementation ensures enhance maximum accuracy and manufacturing convergence. Design teams will be able to concentrate on meeting design specifications as opposed to manufacturing issues. Working with foundry partners is the key to enabling accuracy inside yield analysis tools. Design teams who use tools that incorporate qualified process information obtain the most accurate post-route yield analysis, in addition to the most 'correct by construction' designs.



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Dr. Kuo Wu is Deputy Director of EDA and Design Services Marketing at TSMC. Kuo received his BS, MS and PhD all in Computer Science from Tamkang University, UC Berkeley and UCLA respectively.

Dr. Wu started his career as a VLSI designer at Xerox Corporation. Subsequently he spent most of his career in EDA industry where he served in various technical and business management positions in EDA companies including Silicon Compilers, Meta Software, TSSI, Summit Design, Ambit Design, Cadence and Magma. He was a co-founder and president of an office product company where he created a product from inception to production and won nomination for the Best of Comdex Award.

Dr. Wu, published over a dozen technical papers and is the holder of several US patents and was an invited lecturer of VLSI design graduate course at USC.



Marilyn Adan

Marilyn Adan is the Senior Technical Marketing Manager for Physical Verification at Synopsys. Her key responsibilities include gathering technical requirements for physical verification and other DFM related technologies. She is also heavily involved in business and sales development for the Silicon Engineering Group.

Before her four year tenure at Synopsys, Marilyn was involved in the high-tech. field for nearly twenty years working in numerous areas, including design methodology creation and chip design at Raza Foundries, management of a team of application consultants at Avant!, and manufacturing development at Hewlett Packard.

Marilyn has a BSEE and MSEE from San Jose State University. She has published a number of technical papers and appears as a panelist at various technical conference venues.

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