

# IC Compiler-Advanced Geometry

Comprehensive Place and Route System for 20nm and Below Designs

## Overview

*IC Compiler-Advanced Geometry is the newest addition to the IC Compiler family of products.*

*IC Compiler-Advanced Geometry includes all the capabilities of IC Compiler plus features specifically targeting design nodes at 20nm and below. It provides best-in-class quality of results (QoR), strong signoff correlation, and enhanced manufacturability for today's most advanced designs.*

## IC Compiler-Advanced Geometry

IC Compiler-Advanced Geometry is an integral part of the Synopsys Galaxy™ Implementation Platform. IC Compiler-Advanced Geometry (IC Compiler-AG) is a single, convergent, chip-level physical implementation tool that targets designs at advanced technology nodes of 20nm and below. It encompasses all the capabilities of IC Compiler including flat and hierarchical design planning, placement and optimization, clock tree synthesis, routing, design for manufacturing, and low power capabilities.

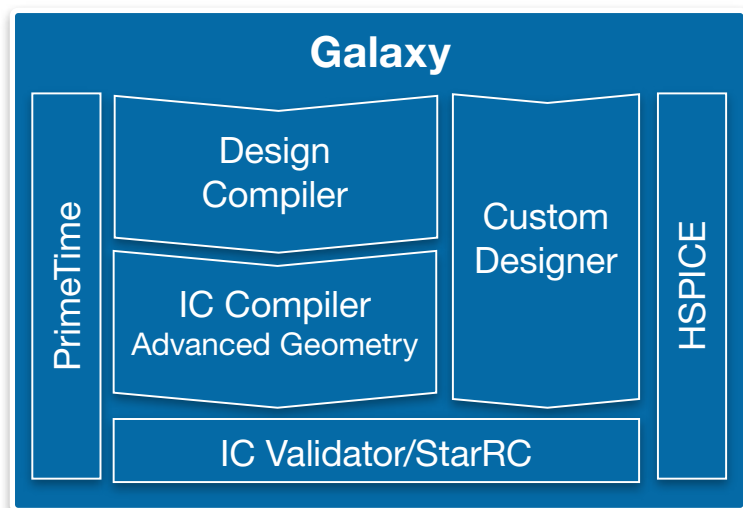


Figure 1: Synopsys Galaxy Implementation Platform

## Physical Implementation for Advanced Geometries

IC Compiler-Advanced Geometry delivers specific solutions to address the key technology challenges presented by the 20nm process node and below.

These include support for foundry design rules at 20nm and double patterning technology (DPT) awareness throughout the flow. This enables faster timing and DRC closure while minimizing the area and power of your design.

- ▶ Comprehensive manufacturing aware technology concurrently optimizes for yield with timing, area, power, test, and routability. IC Compiler-Advanced Geometry increases manufacturability of the design, optimizing both functional and parametric yield. Zroute technology prevents and fixes DPT violations while providing the fastest DRC closure and highest manufacturability.
- ▶ In-Design physical verification with IC Validator enables fast signoff-quality DRC and DPT decomposition checking within the implementation

environment. Intelligent integration with IC Compiler-Advanced Geometry makes it possible for designers to identify and automatically repair corner case violations, eliminating late stage surprises and accelerating design closure for manufacturing.

## Quality of Results

Innovative technology in IC Compiler-Advanced Geometry takes into account the impact of moving to smaller technology nodes. It delivers improved QoR, measured in terms of the complete cost vector — timing, area, power, signal integrity, routability, and yield. DPT-aware placement and global route improves congestion modeling early in the flow to provide the best possible area.

- ▶ DPT Enablement: Double patterning requires decomposing the routing patterns into alternating red and blue colorized optical proximity correction (OPC)-aware photo lithography masks. Each mask is exposed separately and the resulting exposure correctly captures the design intent as shown in figure 2.

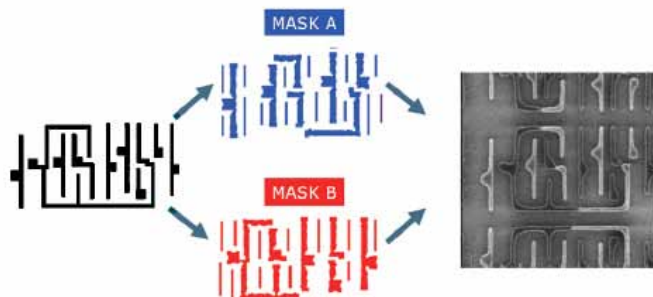


Figure 2: Double patterning mask colorization

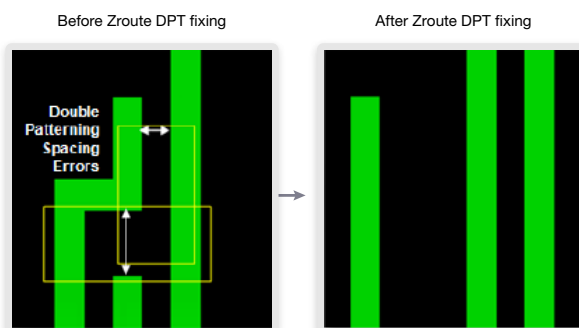


Figure 3: Double patterning aware routing

IC Compiler-Advanced Geometry's DPT technology uses a strategy of cell library preparation, placement, and routing to achieve the highest quality layout result while inherently understanding and implementing DPT requirements.

- ▶ DPT-Aware Placement: Observes the library-specified double patterning spacing requirements during placement. DPT-aware placement ensures that there are no DPT violations due to cell adjacency.
- ▶ DPT-Aware Routing: Handles double patterning effects comprehensively through the IC Compiler-Advanced Geometry flow to significantly reduce the impact on the physical designer. As shown in figure 3, the router handles DPT effects throughout physical implementation with the global router modeling the impact of double patterning on congestion and the detail router understanding all the DPT rules, thus avoiding "odd cycles" through the design flow.
- ▶ Advanced Routing Technology: Handles today's complex design rules and soft rules efficiently. Zroute technology understands 20nm design rules leading to faster DRC convergence. Examples of some of these advanced design rules that have been implemented are shown in figure 4.
- ▶ Extraction: Correlates with the industry-standard signoff extraction tool, StarRC™. It models the appropriate 20nm effects during implementation, such as orientation-based width bias.
- ▶ DPT Compliance: In-Design physical verification with IC Validator and IC Compiler-Advanced Geometry provides DPT compliance checking, allowing designers to quickly identify and repair corner case DPT violations.

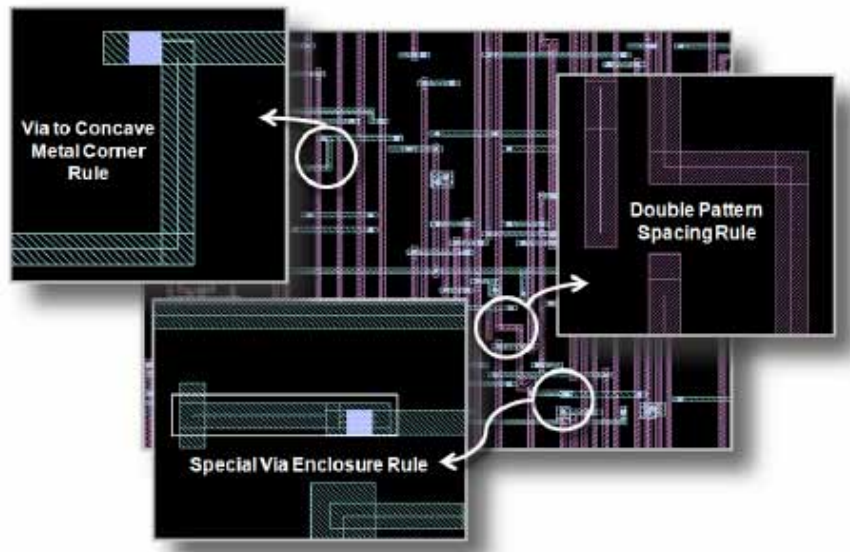


Figure 4: Examples of 20nm rule support

## Turnaround Time

IC Compiler-Advanced Geometry provides the fastest path to DRC and DPT clean results. This is achieved by using the best-in-class hierarchical design planning, placement, clock tree synthesis and routing core engines to handle DPT requirements comprehensively. The built-in algorithms make automatic tradeoffs to give the fastest design convergence while minimizing the area impact.

- ▶ Design Planning: Includes complete flat and hierarchical design planning capabilities delivering multi-million-instance design capacity within a single environment.
- ▶ Correlation to Signoff: Tight correlation to industry standard signoff tools, PrimeTime® SI and StarRC™ is included. IC Compiler-Advanced Geometry shares delay calculation models with PrimeTime and PrimeTime SI, including cell delay, Arnoldi wire delay, composite current source (CCS) models, as well as features like clock reconvergence pessimism removal (CRPR) and on-chip variation (OCV) to achieve the highest correlation to signoff in the industry.

- ▶ Design Convergence: There are a number of design links with other industry standard Synopsys Galaxy Implementation Platform products that facilitate fast design convergence. IC Compiler-Advanced Geometry, in combination with Design Compiler® Graphical, provides the industry's strongest correlation between synthesis and physical implementation which minimizes placement congestion. Signoff-driven signal integrity (SI) closure with PrimeTime SI and StarRC provides productivity benefits. In the final stages of design closure, IC Compiler-Advanced Geometry utilizes PrimeTime SI and StarRC to incrementally deliver signoff-assured design results within the implementation flow. In-Design physical verification with IC Validator and IC Compiler-Advanced Geometry accelerates design closure for manufacturability by enabling signoff quality checking and automatic repair within place and route.

- ▶ Multi-Corner Multi-Mode (MCM): Concurrent MCM-aware placement, routing, and optimization transformations dramatically reduce turnaround time for large, complex chips with multiple modes and corners. Intelligent optimization is driven by timing, area, power, signal integrity, routability, and yield cost factors that are measured concurrently across all scenarios.
- ▶ Zroute Technology: Zroute technology in IC Compiler-Advanced Geometry utilizes advanced routing algorithms and multithreading capability to take full advantage of the newest multicore computer platforms, delivering up to 10x speedup with mainstream platforms. The Zroute architecture incorporates state-of-the-art routing technology, such as native soft rules to enable lithography-aware routing and avoid manufacturing problems. Employing concurrent optimization techniques, Zroute simultaneously considers the impact of manufacturing rules, timing, and other design goals to deliver high QoR along with improved manufacturability.

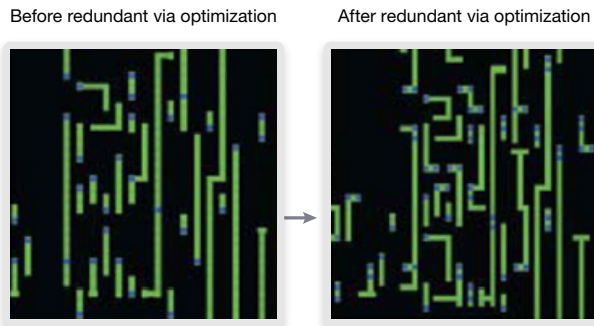


Figure 5: Zroute redundant via optimization

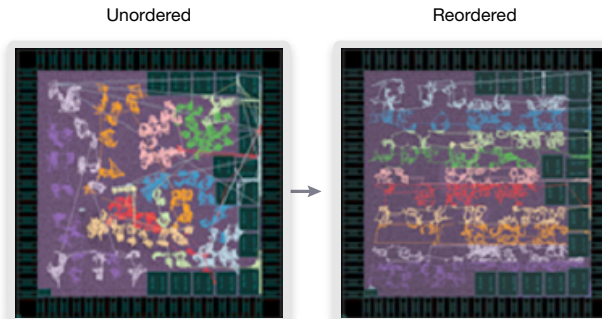


Figure 6: Scan chain reordering

## Cost of Design

IC Compiler-Advanced Geometry allows designers to utilize a variety of techniques to meet timing, power, area, routability, and yield goals while considering the effects of double patterning during the flow. This reduces the cost of design by working to minimize the area impact of DPT and increases design closure predictability.

- ▶ **Manufacturing Awareness:** The only complete solution available to optimize for yield and manufacturability. Concurrent optimizations maximize the use of redundant vias, reducing the number of remaining single vias (as seen in figure 5) and the critical area for higher yield, while still meeting timing QoR.

- ▶ **Low Power:** Power management has become an extremely important design issue. Advanced multivoltage designs for wireless, mobile, and consumer applications must deliver maximum performance while minimizing power. IC Compiler-Advanced Geometry and the Synopsys Galaxy Implementation Platform support UPF (IEEE 1801) to deliver a complete low power flow that handles complex power-sensitive applications.
- ▶ **Design for Test (DFT):** IC Compiler-AG, along with DFTMAX™, provides a comprehensive test automation solution that offers SoC designers the fastest and most cost-effective path to high-quality manufacturing tests and working silicon. Figure 6

highlights the IC Compiler-Advanced Geometry scan chain reordering technology. Fully-integrated DFTMAX next-generation test compression and synthesis technology, achieves high compression without affecting the test coverage, functionality, timing, or power requirements of the design.

Key advances in IC Compiler-Advanced Geometry along with links to other Synopsys Galaxy Implementation Platform products allow IC Compiler-Advanced Geometry to deliver the best QoR in terms of timing, area, power, routability, testability, and yield, as well as faster turnaround time and a predictable path to first-silicon success. IC Compiler is the industry standard, production-proven, place and route tool of choice for today's toughest and most complex designs. With its advanced node design rule support and new DPT features, IC Compiler-Advanced Geometry extends Synopsys physical implementation to 20nm and below.

**For more information about IC Compiler-Advanced Geometry please contact your local sales representative or visit us at [www.synopsys.com](http://www.synopsys.com).**