28nm Silicon And Design Enablement

The Foundry And EDA Vendor Perspective

JC Lin
Vice President R&D
IC Compiler

synopsys
Today
IC Compiler 32/28nm Webinar Series

- Done
  - 32/28nm Design Challenges
- Done
  - Addressing 32/28nm Design Challenges
- Done
  - Fastest Time to Tapeout with IC Validator
- Done
  - Realizing Today’s 32nm and Beyond Large Designs
- Done
  - Manufacturing-Aware Routing
- Done
  - Extraction For 32/28nm

Today’s Topic
28nm Silicon And Design Enablement A Foundry And EDA Vendor Perspective
Welcome!

JC Lin
Vice President, R&D
IC Compiler
Synopsys
32/28nm Design Enablement

Overview of Synopsys Solutions At 32/28nm

- Featured Technologies
  - In-Design STA: Final-stage Leakage Recovery
  - In-design physical verification: Automatic Litho-repair Using Pattern Matching Technology
Synopsys Solutions At 32/28nm

- **Variability**
  - High accuracy
  - MCMM throughout the flow

- **Enhanced Manufacturing Compliance**
  - Routing, Physical Verification & Test

- **Low Power**
  - Comprehensive flow
  - Major advances in 2010.03 and 2010.12

- **Design Complexity**
  - Runtime speedup
  - 40M+ design handling

**Production proven across 32/28nm process nodes**
Leading The Way In Tapeouts At 32/28nm

First to 45nm, First to 32nm

@ 32/28nm
High Accuracy Flow Reduces Margins
Critical For Convergence At 32/28nm

Device & Delay Models

RC models & Net Topology

Advanced OCV

Composite Current Source Models (CCS)

Driver Model

Reduced Order Network Model

Receiver Model

- NLDM
- CCS
- Elmore
- Arnoldi
- NLDM
- CCS

Output current waveform in library

Current vectors

slew

0.1

0.2

0.3

0.4

0.5

0.6

0.7

Output cap

0.023

0.047

0.065

0.078

0.091

Reduced Order Network Model

Driver Model

Receiver Model

• NLDM
• CCS
• Elmore
• Arnoldi
• NLDM
• CCS

Advanced OCV

Delay

140

120

100

80

60

40

20

1 stage

2 stages

3 stages

4 stages

5 stages

6 stages

Depth

1

2

3

4

5

6

Derate

1.2

1.2

1.15

1.15

1.08

1.08
Concurrent Multicorner Multimode
Reduces Uncertainty At 32/28nm

Multicore Support

Full Flow MCMM with SI

Design Compiler
Design Planning
Placement
CTS
Routing

Comprehensive MCMM support - faster TAT, best QoR and easy to use
Enhanced Reliability At 32/28nm

Preventative EM & Integrated IR Flow

Electromigration
Aware CTS

In-Design PrimeRail
IC Compiler Integration

User provided
X-Y padding

Before EM-Aware CTS

After EM-Aware CTS

Logic cell

Logic cell

Clock cell

Error Browser identified missing via

Based on guidance IC Compiler adds in the missing via

Comprehensive flow addresses EM & IR issues
Comprehensive Low Power Flow

Multi-Voltage And UPF Support

MV Support

- Auto-insertion of LS/ISO cells
- Disjoint VA and Always-On Synthesis
- MV-aware power network synthesis
- MTCMOS power gating

Improved Productivity - UPF

Multi-voltage Aware Opt.

Production proven automated flow produces best QoR
**Low Power CTS**

*Complete Support At 32/28nm*

**New In 2010.12**

- Smart selection of buffers vs. inverters
- Power driven sizing
- Intelligent clock net layer selection
- Target transition relaxation

= 10% reduced power OOTB

**XOR Clock Gating**

Extra 10% reduced power

**Datapath For CTS**

Datapath ICG placement & routing ~30% less power

Significant clock tree power savings for high-performance designs
Best Leakage QoR
MCMM Aware, Handles More VTs

MCMM Throughout

On average 7% better leakage

Physical Flow

Optimizing leakage and other costs through the flow

In-Design STA

Delivers Maximum Leakage Savings

Final-stage Leakage Recovery

Better leakage and timing - faster convergence at 32/28nm
Faster Design Exploration
20M Instances In One Day

Exploration Placement
Coarser placement no legalization
25M instances in 1 hour

Faster Global Route
Global routing results
see top-level congestion early

Virtual IPO
Provides early look at timing QoR

2X Faster initial floorplan creation
Feasibility Flow
Faster & Easy To Debug

Check & Report
- User customizable
- “What Next” recommendations

Feasibility Optimization
- 2X faster place_opt & 1.5X clock_opt to assess dirty SDC

Categorized Reports
- HTML links to reports and/or GUI for debug

Increased designer productivity in the early stages of the design
Faster Hierarchical Design Planning

On Demand Loading Technology

On-Demand Loading

Original netlist
1.8M Cells

Removes internal logic within partitions to place & optimize interface logic

Top-level Designers View

On-demand netlist
50K Cells

Top level design has the top level and interface cells to route & time (GUI)

2.8X runtime and 2X memory improvement
32/28nm Rule Formulation & Support

**Placement Rules**

- 2x: Standard Cell
- 1x: Filler Cell

**Routing Rules**

Example: 3-neighbor, end-of-line via-enclosure rule

**Soft Rules**

Soft rule for wire spacing

Yield vs. spacing plot

Supported by leading foundries and major IDMs
Zroute – Manufacturing-Aware Router

Tapeout Proven At 32/28nm

Core Technology

Realistic Connectivity

Virtual Wire

Dynamic Maze Grid

Manufacturing Compliant

Redundant Vias

Wire widening & spacing

Litho friendly routing

Multicore Delivers 3X Speed-up

3X Speed-up, higher QoR, better manufacturability
In-Design Physical Verification

*Improved Productivity For The Physical Designer*

**In-Design DRC**
- Auto-Repair
- Signoff Quality
- Incremental

**In-Design Metal Fill**
- Timing-Aware
- 10x Faster
- Highest Density

**In-Design LCC**
- Featured Technology
- Automatic litho-repair using pattern matching
32/28nm Design Enablement

- Overview of Synopsys Solutions At 32/28nm

- Featured Technologies

  In-Design STA: Final-stage Leakage Recovery

  - In-design physical verification: Automatic Litho-repair Using Pattern Matching Technology
Leakage Trends At Advanced Nodes

- Sub-threshold leakage current dominates total leakage power
- Advanced nodes require new techniques
  - Leakage QoR with leakage variants (eg. Channel-length variation, multi-Vt)
  - Managing increasing leakage variability

Need to approach leakage optimization from a device modeling perspective
Leakage QoR With Leakage Variants

Channel-Length Variation, Multi-Vt Libraries

- Increasing channel length is also referred to as CD biasing
- Besides Vt variants, leakage reduction is possible by increasing gate length
- Potential foot-print equivalent leakage variants in standard cell libraries

Example: 3 different leakage variants of a NAND3 with CD biasing

Significantly reduced impact on top-pin-to-out timing with considerable leakage reduction

No impact on most timing with some leakage reduction

For most effective leakage reduction
In-Design STA -- Final-Stage Leakage Recovery

• Architected for 15+ channel-length based leakage variants and Vt libraries

• Used on “final” netlist for leakage recovery
  • Reduces leakage while preserving signoff timing/DRC
  • Minimal physical perturbation

• Driven by PrimeTime® STA

• Augments leakage savings delivered by standard leakage flow in IC Compiler

% Leakage recovery depends on how much power optimization was done earlier in flow
32/28nm Design Enablement

• Overview of Synopsys Solutions At 32/28nm

• Featured Technologies
  – In-Design STA: Final-stage Leakage Recovery
  – In-Design Physical Verification: Lithography Hotspot Prevention Using Pattern Matching
Manufacturing Challenges at 32/28nm

Sub-Wavelength Gap

- Poor process printability

More & More Rules

- Difficult to write and maintain

Complex Feature Dependencies

- Beyond nearest feature

Address Lithography Limiting Patterns During Design
In-Design PV – Litho Hotspot Prevention

Built on Patented Pattern-Matching Technology

- Prevent
- Match
- Repair

<table>
<thead>
<tr>
<th>IC Compiler (ICC)</th>
<th>IC Validator (ICV)</th>
<th>ICC+ICV</th>
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<tbody>
<tr>
<td>• Manufacturing aware routing avoids litho hotspots</td>
<td>• Pattern-matching based detection of lithography limiting layout patterns</td>
<td>• Automatic repair and revalidation of matched layout patterns</td>
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Fastest Path to Litho-Clean Design Closure
In-Design PV – Pattern-Matching

Patented Technology Enables Fast Litho Detection

Automated Pattern Capture
- Directly from OPC, LRC or Simulation

Intelligent Layout Filtering
- Fast Identification of Match Candidates

Database-Driven Pattern Matching
- Zero Runtime Penalty per Pattern

Qualified by GlobalFoundries for 28nm Process
In-Design PV – Auto Litho Repair

Smart Integration Eliminates Corner-Case Patterns

Highly Localized

Router-Driven

Incremental Validation

Negligible Physical Impact

Full Property Visibility

Timing Aware

Proven Algorithms

Highest Quality Final Layout

4-5x Faster Analysis

Eliminates Need for Manual Layout Fixes
Results: Automatic Litho Repair

Customer Designs, 45/40nm

High Repair Rate

- Before
- After
- Repair Rate

<table>
<thead>
<tr>
<th>Design Instances</th>
<th># Litho Hotspots</th>
<th>Repair Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>617k</td>
<td>187</td>
<td>80%</td>
</tr>
<tr>
<td>966k</td>
<td>457</td>
<td>85%</td>
</tr>
<tr>
<td>2.4M</td>
<td>1214</td>
<td>90%</td>
</tr>
</tbody>
</table>

Fast Runtime

- Detection
- Repair
- Patterns in DB

<table>
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<tr>
<th>Design Instances</th>
<th>Runtime (min)</th>
<th># Patterns</th>
</tr>
</thead>
<tbody>
<tr>
<td>617K</td>
<td>617K</td>
<td>1</td>
</tr>
<tr>
<td>966K</td>
<td>966K</td>
<td>10</td>
</tr>
<tr>
<td>2.4M</td>
<td>2.4M</td>
<td>100</td>
</tr>
</tbody>
</table>

Hotspot Free in Minutes
Synopsys Solutions At 32/28nm

Summary

Variability
- High accuracy
- MCMM throughout the flow

Manufacturing Compliance
- Routing, Physical Verification & Test
- In-Design PV: Litho Hotspot Prevention using Pattern Matching

Low Power
- Comprehensive flow
- Low Power CTS
- In-Design STA: Final-stage Leakage Recovery

Design Complexity
- Runtime speedup
- 40M+ design handling

Production proven across 32/28nm process nodes
Thank You!

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Predictable Success

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