IC Compiler: Routing, DFM

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Outline

• About Intel
• Design Rules and Routing
• Design For Manufacturability (DFM)
• Summary
About Intel

• World’s largest semiconductor company
• First with 45nm production silicon
• 32nm logic process with a functional SRAM demonstrated

Source: http://www.intel.com/technology/architecture-silicon/32nm/index.htm
Design Rule Trend

Growth in Number and Complexity of Rules

- Significant increase in the Number and Complexity of design rules in DSM Processes
- The rule complexity is moving up the layer stack

Source: Layout rule trends and effect upon CPU design
Process Dependence

• In lithography, 193nm light used to print geometries smaller than 193nm
  – Pattern Fidelity
  – Rules depend on adjacent geometries
  – Width dependent Spacing, Forbidden-pitch

• Chemical Mechanical Polishing in Cu causes non-uniform interconnect sheet resistance and capacitance across the die
  – Rules to provide a uniform environment for wires
  – Rules to keep wire and via reliable
IC Compiler Routing

• Different spacing in orthogonal directions
  – nonPreferredRouteMode
• Line-end and line-side spacing per metal layer
  – M<n>EolTip2SideSpacing (n=1..max_layer)
• Multiple min edge length and stub length modes
• Strict On Grid Design
  – noOffGridRouting, noOffsetFatVia, V<n>NoOffGridRouting
• Complex Via Spacing Rules
• IC Compiler Router supports 45/32nm rules
  – Maximally design rule clean layout
IC Compiler Rule Support Example

• A 45nm Stub mode

- If a metal has width of $W < Q$ (stubThreshold) and there is no connecting metal within $W_{\text{min}}$ (minWidth), and has neighboring metal along two adjacent edges (any one edge < L distance from the corner of two adjacent edges), then one of the spacing ($S_1$ and $S_2$) should be $\geq S_e$; Neighboring metal is searched from corner to distance of $K$. 

Source: SNPS ICC Advanced Rule Support, 2008
DFM

- DFM defines modes/methods for Design and Manufacturing for improving Yield
  - Geometrical Design, Electrical Design, Variability
- DFM as a solution – a set of methodologies for mitigating “variability”
  - Tight link to co-optimize product, design, process

DFM in the Design Flow

Design Collaterals
- Layout Rules
- Electrical Rules
- Standard Cell Library

DFM Rules, Guidelines, Constraints
DFM Aware Cell Layout; Regularity
Cell Layout Optimized for RET Methods
Supports Block Level DFM Methods

Floorplan & Power Network Design
- Redundant Via in Power Grid
- Regular Power Grid

Logic Synthesis
- Choice of DFM friendly cells

Placement
- Abut Rules for Cell Placement
- DFM Rules for Macro Placement

Routing
- DFM Aware Routing
- Regular Routing Grid
- Post Process for Clean DFM/Fill

Extraction and Timing
- Fill Aware Extraction
- XCAP with Fill

Layout Completion
- Fill (Planarity and Density)
- DFM Cleanup,

Layout Verification
- Check and Sign-off
DFM in IC Compiler Design Flow

**Design Collaterals**
- Layout Rules
- Electrical Rules
- Standard Cell Library

**Floorplan & Power Network Design**
- DFM Rules, Guidelines, Constraints
- DFM Aware Cell Layout; Regularity
- Cell Layout Optimized for RET Methods
- Supports Block Level DFM Methods

**Logic Synthesis**
- Choice of DFM friendly cells

**Placement**
- create_fp_plan_group_padding
- set_keepout_margin, set_cell_padding

**Routing**
- corner and jog reduction, via rotation, EOL Spacing, Complex Via Rules

**Extraction and Timing**
- set_tiu_plus_files with fill emulation, cap scaling

**Layout Completion**
- insert_fill, insert_metal_filler
- insert_redundant_via, insert_spare_cells

**Layout Verification**
- Check and Sign-off
Summary

• Design Rule Complexity is increasing with newer process generation
  – IC Compiler router supports complex 45nm/32nm Design Rules

• DFM principles has to be applied through the entire design flow
  – DFM is not a point tool, it is one of the solutions to mitigate variability
  – Discussed a DFM centric IC Compiler Design Flow