FPGA Design Solutions for Military and Aerospace Applications

- High Reliability
- Technology Independence
- High Performance Through Optimization
- Used in DO-254 Compliance
- High-Level RTL Synthesis
- Fast Debug and Verification
High-Reliability Implementation Solutions for Military and Aerospace Applications

Hardware designers targeting military and aerospace applications have special requirements that demand highly reliable design tools and methodologies that enable them to meet their design goals and operational safety without compromising performance. Applying its years and breadth of design tool expertise, Synopsys delivers high-quality, high-performance and technology-independent solutions developed to address the unique needs and parameters of Mil/Aero and other high-reliability applications. Synopsys’ tools and methodologies for FPGAs that ultimately end up in space or other harsh operating environments enable you to develop a reproducible requirements-driven design process including system specification, RTL coding, logic synthesis and verification. Used for implementation of DO-254 processes to meet FAA standards and ensure the safety of airborne hardware, Synopsys’ FPGA design and verification tools have been used in many successful projects, such as the Mars Rover and critical systems in military aircraft.

“Microsemi has served military and space customers for decades by delivering leading edge reliability, lowest power, and the most secure programmable logic devices available. Our customers use Synopsys’ best-in-class FPGA synthesis and debug solutions to maximize their productivity,”

Esam Elashmawi
Vice President and General Manager at Microsemi

High-Reliability Design

Synopsys Synplify® Premier and Certify® software incorporate several advanced optimization techniques to address high-reliability requirements such as single-event upset (SEU) detection and mitigation, fault-tolerant state machine encoding and support for inference of error correcting (ECC) memory.

Triple Modular Redundancy (TMR)—Synplify Premier software can automatically implement user-selected logic in triplicate and add the associated voting logic to determine the correct state.

Error Correcting Code (ECC) Memories with TMR—ECC with TMR can be used for single bit error detection and correction in memories by preventing false data from being captured in memory and being propagated to other parts of the design.

Safe State Machine Encoding—Synplify Premier and Synplify Pro® FPGA design software allows you to specify an attribute that tells the tool to use safe state machine encoding algorithms to produce a highly reliable implementation of the state machine in your design.

Fault-Tolerant FSMs with Hamming-3 Encoding—in the Synplify Premier tool, users can designate that they wish certain FSMs to use Hamming-3 encoding for the automatic detection and correction of single-bit errors.

Automated Documentation—The HDL Analyst tool, built into Synopsys’ Synplify synthesis solutions, automatically produces highly readable schematics from your HDL source at both the RTL and gate level that may be used for code analysis and professional documentation of your design.

Support for Legacy FPGA Devices—The long life cycles associated with many Mil/Aero applications demand that design software and FPGA parts be archived for potential future use. Synopsys offers archive licenses of software for this purpose and typically offers synthesis support for mature devices, longer than is supported by FPGA vendor software.

DO-254 Support

The RTCA/DO-254 standard enhances safety in airborne electronic systems and is comprised of five levels of stringency, levels A to E, which are based on the effect of the failure of the hardware upon an aircraft. The Synplify family of high-performance, technology-independent implementation & debugging solutions are designed to aid DO-254 compliant processes for FPGA development. In addition, accurate functional verification against initial requirements is a critical component of meeting DO-254 standards. A Synopsys verification flow, using the VCS® RTL verification solution coupled with the Verification Methodology Manual (VMM) techniques promote the creation, execution and measurement of a complete verification plan. Prototyping can be an important step in verifying DO-254 compliance and Synopsys provides a comprehensive FPGA-based prototyping solution that enables hardware-based verification for both ASIC and FPGA-based systems. These tightly integrated, easy-to-use products facilitate complete system debugging, testbench execution and early software development.
“Designs targeted for military and aerospace applications require the highest level of quality and reliability. The combination of Xilinx defense-grade and space-grade FPGA families and Synopsys production-proven FPGA synthesis products offer designers not only the best performing devices, but more importantly, high reliability and quality.”

Yousef Khalilollahi
Sr. Director, Aerospace & Defense, Xilinx, Inc.

High-Level Synthesis
Synopsys also provides high-level synthesis (HLS) tools that achieve greater design and verification productivity from algorithmic concept into silicon. Synphony™ C Compiler and Synphony Model Compiler provide optimized implementation paths from C/C++ and high-level, fixed-point models into RTL. Both products provide HLS optimization technologies that deliver high quality of results for FPGAs and ASICs, and enable rapid exploration of performance, power and area tradeoffs. With the Synphony tools, users can specify designs at a very high level of abstraction using C/C++ languages or IP model libraries and then use the Synphony HLS compilers to create optimized RTL and testbenches for ASIC and FPGA designs, FPGA-based and virtual prototyping and for verification using C or RTL.

RTL Verification and FPGA-Based Prototyping
Synopsys offers the VCS functional verification and debug environment, enabling chip and system developers to find and fix critical design defects as early as possible to avoid schedule delays and keep production costs to a minimum. VCS, along with the VMM methodology, supports a DO-254 compliant RTL verification solution. Synopsys’ HAPS® FPGA-Based Prototyping Solution enables pre-silicon software development and hardware/software integration of both subsystems and complete systems at near real-time speeds using real-world interfaces. Software development and system validation teams will benefit from improved productivity and a reduction in the overall product development schedule. The complete solution consists of the HAPS FPGA-Based Prototyping hardware supported by an integrated tool flow including Synplify FPGA synthesis software, Certify multi-FPGA ASIC prototyping software and the Identify® RTL Debugger. Synopsys’ FPGA-based prototyping solution is ideal for demanding validation environments where real-world interfaces and large test suites are essential.

“Microsemi customers using our DSP capabilities enjoy the benefits of using the Synphony Model Compiler within our Libero design flow to perform architectural optimizations from Simulink specifications.”

Jim Davis
Vice President, Software & Systems Engineering at Microsemi

“Military and Aerospace customers require the highest reliability along with state-of-the-art programmable capabilities. Altera designs FPGAs, ASICs and CPLDs to meet these exacting standards while offering solutions for a broad set of Military and Aerospace applications. Altera partners with Synopsys to give customers a choice of design tools with the industry-standard Design Compiler flow, Synphony C-code tools and high-reliability development capabilities throughout their tool set.”

Ian Land
Senior Manager, Military Business Unit at Altera Corporation