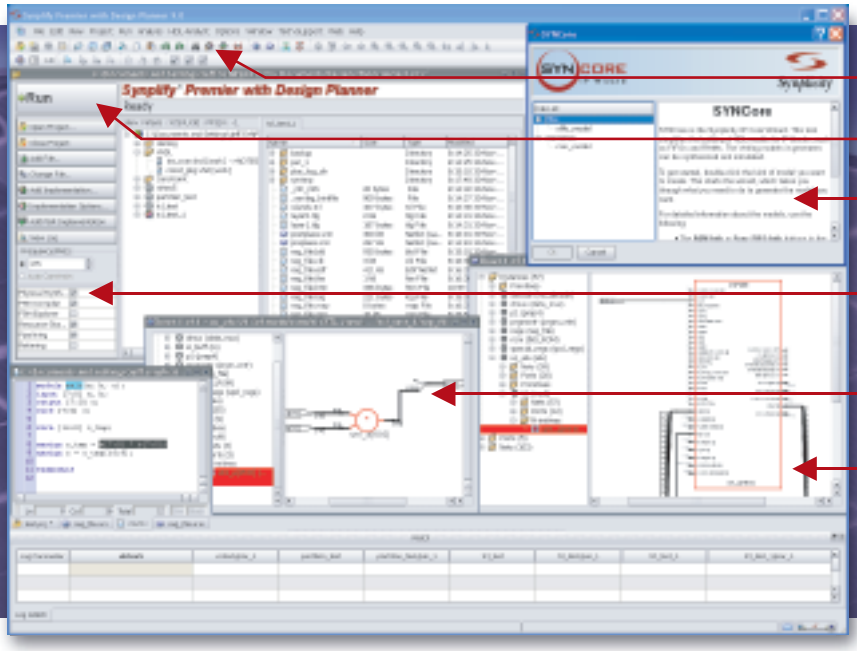
Synplicity
Simply Better Results

Synplify® Premier

Part Of The Confirma™ ASIC/ASSP Verification Platform

The Ultimate in FPGA Implementation and Debug



- Integrated RTL debug for real time FPGA verification
- True timing-driven FPGA synthesis
- Automatically generate technology-independent RTL for memories and FIFO
- Single-pass, fully automated physical synthesis for fast timing closure
- Automatically generated RTL block diagram for analysis
- DSP-friendly synthesis algorithms

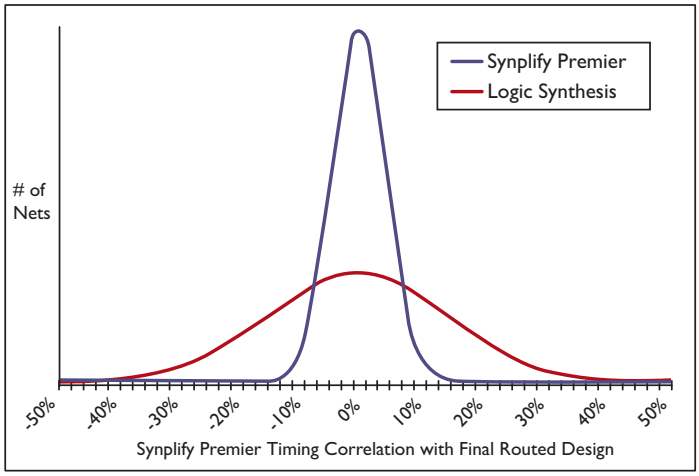
The Synplify Premier software from Synopsys' Synplicity Business Group is the ultimate FPGA synthesis and debug environment. It provides a comprehensive suite of tools and technologies for advanced FPGA designers as well as ASIC prototypers who are targeting a single FPGA.

The Synplify Premier solution addresses the biggest FPGA design challenges including timing-closure, logic verification, IP usage, ASIC compatibility, DSP implementation, and debug while providing tight integration with FPGA vendor back-end tools.

Graph-Based Physical Synthesis For Faster Timing Closure

Today's high density FPGAs make it increasingly difficult for designers to meet their aggressive timing goals quickly. The Synplify Premier software addresses this challenge with its patented Graph-based physical synthesis technology. Synplicity invented Graph-based physical synthesis to improve timing closure by representing preexisting wires, switches, and placement sites within an FPGA as a detailed routing resource graph and then using this graph alongside Synplify Premier's synthesis algorithms to merge optimization, placement, and routing into a single process. This methodology results in timing estimations that are highly correlated with final post-P&R timing. Having highly accurate timing during logic optimization ensures the correct critical paths are being optimized, significantly reducing design iterations and shortening development time.

Accurate Timing Estimation - Superior Timing Correlation
90% of critical paths within +/- 10% of actual value



Accurate timing estimation during synthesis is the key to faster timing closure. The Synplify Premier algorithms combine placement, optimization, and routing to achieve unprecedented estimation accuracy. This facilitates accurate critical path identification, optimization, and placement, improving performance up to 20% and drastically reducing the number of iterations required to meet timing goals.

Synplify Premier Features	Benefits
Graph-based Physical Synthesis	Fast timing closure and a push-button performance boost of up to 20%.
True Timing-Driven Synthesis	After meeting timing constraints, automatically optimizes your design for area/cost.
Technology Independence	Target popular FPGAs from a single RTL and constraint source.
Comprehensive Language Support	Supports Verilog, VHDL, System Verilog, and mixed-language designs.
Automatic Handling of DSP Functions	Infers DSP functions from RTL and maps into vendor's DSP hardware (i.e. MACs, DSP 48).
Lightning-Fast Compile Times	Synthesizes even the largest design in a fraction of the time of other tools.
HDL Analyst® RTL Analysis and Debugging Tool	Generates an RTL block diagram from your RTL code for graphical design analysis and cross-probing.
Interactive Timing Analysis	Enables point-to-point timing analysis without re-synthesis.
Automatic RAM Inferencing	Bypass tedious hand instantiation of RAM and makes your design technology independent.
Graphical State Machine Viewer	Fast debugging and documentation of state machines in your design.
FSM Explorer	Automatically finds and selects the best FSM coding style for meeting your timing and area constraints.
Automatic Retiming	Moves registers automatically within combinatorial logic to balance delay and improve performance.
SCOPE® Constraints Editor	A single location for expressing and managing design constraints.
Integrated RTL Instrumentation and Debug	Instrument and debug your design directly in your RTL source code.
Incremental RTL Debug Flow	Re-instrument your design without re-running synthesis or place and route.
DesignWare®-compatible Library	Easy ASIC code migration into an FPGA for prototyping.
Automatic Gated Clock and Generated Clock Conversion	Automatically converts gated clocks into FPGA clock enables for efficient implementation.
SynCore IP Wizard	Automatically generates technology-independent RTL for memories and FIFOs

Simulator-Like Visibility Into A Live FPGA

The Synplify Premier software provides a rapid method of finding functional errors in FPGA designs by providing simulator-like visibility into operating FPGA hardware. Synplicity's integrated debugging software, based upon technology from the Identify® RTL Debugger, allows you to annotate signals and conditions you want to monitor directly in your RTL code. Nodes that may be used as breakpoints and watch points are displayed for easy menu-driven instrumentation, and then seamlessly run through synthesis and P&R to implement the FPGA. Once the FPGA has been programmed, the RTL debugger is run, allowing you to view actual signal values from an operating FPGA directly in your RTL code and debug it, in-system, and at the target operating speed. The debugging tool within the Synplify Premier product offers advanced triggering that helps pinpoint design problems that could take a simulator days or weeks to uncover.

DSP Aware Synthesis

DSP functionality within FPGAs continues to rise. The Synplify Premier product automatically infers many DSP functions from RTL code and has DSP-aware mapping technology to take full advantage of the dedicated DSP structures and memories built into today's modern FPGAs. The Synplify Premier product is designed to work seamlessly with Synplicity's ESL synthesis tool, Synplify® DSP.

Single FPGA-based ASIC Prototyping

The Synplify Premier solution is a part of the Confirma™ ASIC/ASSP Verification Platform and offers the most comprehensive system for implementing single FPGA-based ASIC prototypes. The tool's built-in gated clock conversion and Synopsys DesignWare® support enables ASIC code to be implemented into an FPGA without modification. Tight integration with the HAPS™ High-Performance ASIC Prototyping System™ makes prototyping easier than ever.

For multi-FPGA prototypes, the Confirma ASIC/ASSP Verification Platform includes the Certify® implementation tool, the Identify® Pro full-visibility debugging tool, and the HAPS prototyping system. The Confirma platform is ideal for ASIC, ASSP, and SoC design and verification teams who leverage FPGA-based prototypes to avoid costly device respins, expedite software development, and accelerate time-to-market.

Supported Platforms

- Windows Vista & XP Pro
- Solaris
- Linux

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