

Synplify Premier

Fast, Reliable FPGA Implementation and Debug

Overview

The Synopsys FPGA design solution comprises high-quality, high-performance, and easy-to-use FPGA implementation and FPGA debug tools. Designers using the Synopsys FPGA design tools gain fast time-to-results for complex FPGAs, area optimization for cost and power reduction, multi-FPGA vendor support, and incremental and team-design capabilities for faster FPGA design development. The Synopsys FPGA design tools provide additional value by offering DesignWare IP integration, links to high-performance functional verification with VCS, integration with Symphony Model Compiler, and an ASIC compatible synthesis flow for FPGA-based prototyping.

Fast Implementation of Advanced FPGAs and FPGA-Based Prototypes

As part of the Synopsys FPGA Design Solution, Synplify[®] Premier software performs FPGA synthesis for programmable devices sold by Achronix, Altera, Lattice Semiconductor, Microsemi, Silicon Blue and Xilinx. The tool is used by customers designing low-power, high-performance, and high-capacity FPGA-based production systems and high-reliability designs. It is also used by customers who are prototyping ASICs/SoCs using FPGAs, including those using Synopsys' [HAPS[®] FPGA-based prototyping solution](#).

Productivity for Fast Design Turnaround and Fewer Iterations

The Synplify Premier tool delivers rapid runtimes using incremental synthesis flows, fast synthesis mode and automated block-based design. Automatic compile point technology can automatically boost synthesis runtimes by leveraging multiple processors. The continue-on-error feature reduces the number of iterations required during synthesis by continuing the synthesis process even in the presence of erroneous modules, and by generating an error log at the end of the synthesis step. This enables designers to fix all the errors in aggregate at the end instead of restarting the synthesis cycle after each individual error is encountered and fixed.

Team-design features allow design team members to perform parallel and distributed development autonomously, further increasing efficiency. Synplify Premier's path-group technology makes design schedules more predictable by delivering results that are reproducible from one run to the next. Synplify Premier delivers block-based RTL synthesis flows that fully integrate with 3rd party FPGA vendor block-based place-and-route design preservation flows, thereby shortening iteration runtimes, and preserving working, verified parts of the design from one run to the next.

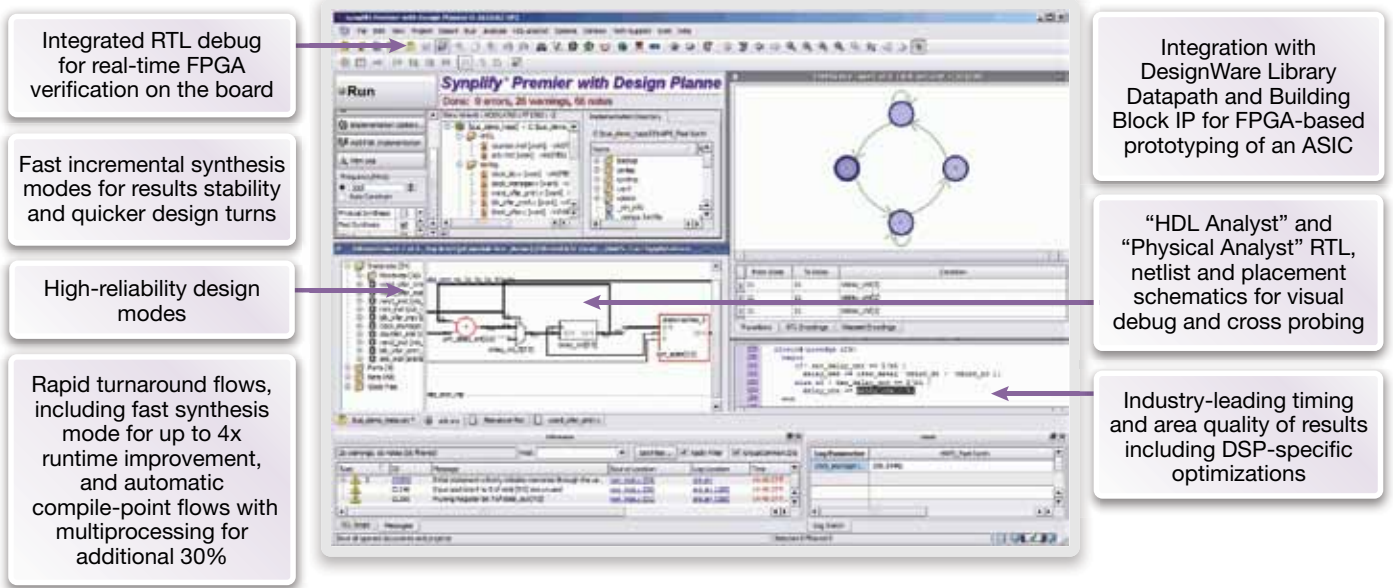


Figure 1: Fast time-to-results for high-performance, high-capacity FPGA designs and FPGA-based prototypes

High-Reliability Design and DO-254 Compliance

The Synplify Premier software provides capabilities to ensure that design processes are traceable, documentable and verifiable. Project files, performance reports, error logs and schematics of ongoing designs are available for documentation. Archive features allow users to take a snapshot of and preserve the design and restore any legacy design at a later date. The tool affords several high-reliability features including the ability to implement Triple Modular Redundancy (TMR) with automatic voting logic and fault-tolerant FSM implementation for automatic error detection and recovery with Hamming-3 encoding or user-specified error recovery. The tool can also infer error correcting code memories and apply TMR in user-specified portions of the design. Additionally, designers can choose to disable certain optimization features to gain greater RTL to netlist traceability.

Power Reduction and Early Power Prediction

The Synplify Premier software includes power optimization algorithms that reduce FPGA power consumption. DSP and memory elements are specifically optimized to allow unused pins to be powered down. Memories are chosen and configured to ensure the lowest power consumption. The Synplify Premier software generates high-quality switching activity data without the need for testbenches and expensive simulation. This activity data can be used by the FPGA vendor’s power estimation tools to estimate overall power consumption early in the design process.

Simulator-Like Visibility Into a Live FPGA

The Synplify Premier software includes the Identify® RTL Instrumentor and Debugger tools to provide an easy-to-use method for finding functional errors in FPGA designs that

are operating on the board. The solution offers simulator like visibility into the implemented FPGA hardware. Using the Identify Instrumentor tool, user’s can annotate in the RTL the signals and conditions that need to be monitored directly. Nodes, which may be used as breakpoints and watch points, are displayed for easy menu-driven instrumentation. Then the user can run synthesis and placement and routing to implement the FPGA with associated monitoring logic. Once the FPGA has been programmed, the Identify RTL Debugger is run, allowing designers to view actual signal values from an operating FPGA, directly superimposed on RTL code. In this way, users can perform in-system debug at the target operating speed.

Signals can be captured and optionally displayed using a waveform viewer. Advanced triggering features help users to pinpoint design problems that take a simulator days or weeks to uncover.

FPGA-based ASIC Prototyping

The Synplify Premier solution offers the most comprehensive set of automated features for implementing FPGA-based prototypes. The tool's built-in gated-clock conversion capability and full integration with the [DesignWare® Library's Datapath and Building Block IP](#) enables ASIC RTL code to be implemented in an FPGA. Tight integration with the HAPS® FPGA-based Prototyping System allows users to quickly implement and debug ASIC prototypes.

Industry-Leading Quality of Results Including DSP-Aware Synthesis

The Synplify Premier product includes enhanced logic synthesis algorithms that provide the best logic synthesis

timing and quality of results in the industry. The Synplify Premier software performs both high-level optimizations as well as detailed optimizations tailored to the specific FPGA architecture and its resources. The Synplify Premier product automatically infers many DSP and memory functions from RTL code and has DSP-aware mapping technology and automatic memory inferencing to take full advantage of each FPGA's unique memory, register and DSP resources. The Synplify Premier product is designed to accept optimized RTL output from the Symphony™ high-level synthesis tool, allowing broad design exploration and faster implementation of DSP and datapath-oriented functions being implemented in FPGAs.

In addition, the user can further improve the quality of results and timing results by using the Synplify Premier product's graph-based physical synthesis technology. The physical synthesis flow generates an optimized, placed netlist in the context of available routing resources, allowing for highly accurate timing estimation during synthesis. This facilitates critical path identification, optimization and placement, improving performance up to 20% and drastically reducing the number of iterations required to meet timing goals.

For more information on the Synopsys FPGA design solution visit www.synopsys.com/FPGA

Synplify Premier Features	Benefits
All of the features in Synplify Pro	The best quality of results and productivity for FPGA design
High-reliability design features	Safe and fault-tolerant FSM implementations with choice of automatic or user-specified error detection and correction
Continue-on-error	Reduces iterations required for board bring-up by identifying multiple errors in one synthesis run
Team design	Faster design iterations and design preservation. Develop your design in parallel and/or in a distributed environment using bottom-up or hybrid bottom-up/top-down flows. No floorplanning required
Physical Analyst	Locate and cross probe to instances/paths within the placed design schematic from your RTL schematic, RTL source file, netlist schematic, netlist file or timing report to better comprehend critical paths
Incremental timing analysis	Point-to-point timing analysis, without re-synthesis, when timing exception constraints are changed
Physical Plus flow	Routing Congestion Reduction and Timing Closure for Xilinx Virtex devices
Automatic handling of Digital Signal Processing (DSP) functions	Infer DSP functions from RTL and map into vendor's DSP hardware (e.g. MACs, DSP 48) for improved QoR
Automatic RAM memory inferencing from the RTL	Better quality of results. Bypass tedious hand instantiation of RAM and make the design technology independent
SynCore IP Generator	Automatically generate technology-independent RTL for memories, FIFOs and arithmetic functions
Comprehensive HDL language support	Verilog, VHDL, System Verilog, VHDL-2008 and mixed-language designs
Incremental RTL debug flow	Re-instrument your design without re-running synthesis or place and route
Integrated RTL instrumentation and debug (Identify tool)	Debug your design directly from your RTL source code using the working FPGA implemented on the board
HDL Analyst	Interactive debug. Efficient constraints setting as well as cross-probing between RTL source code, netlist, RTL schematics, netlist schematics
Automatic gated clock and generated clock conversion	Easier implementation of the ASIC design in an FPGA. Automatically convert gated clocks into FPGA clock for efficient implementation in flat or block-based flows
DesignWare Library support	Easy ASIC code migration into an FPGA for prototyping
Integration with Symphony High-Level Synthesis	Optimally implement DSP and other datapath-oriented designs in an FPGA



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