

Unified Implementation Solution for Digital and Custom SoC Designs

Accelerated SoC Implementation with IC Compiler and Custom Designer

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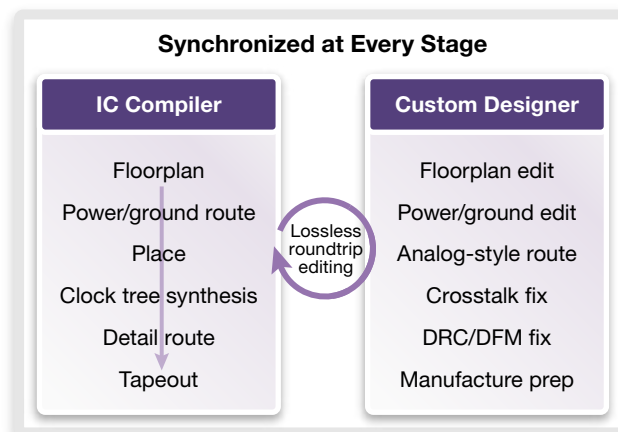
Overview

The Galaxy™ Implementation Platform provides seamless integration between the IC Compiler physical implementation and Galaxy Custom Designer® custom implementation solutions, allowing design teams to easily move between digital and custom implementation flows while maintaining design data integrity. The unified solution accelerates the design development cycle by enabling quick and reliable custom edits to IC Compiler designs at any stage of development, including the time-critical tapeout phase.

Galaxy IC Compiler and Custom Designer Unified Solution Highlights

Many SoC designs require both cell-based and custom physical implementation capabilities to address the challenges created by increased levels of digital and analog integration and high-speed signals. Traditionally, digital place-and-route was accomplished by manually transferring the design to a non-integrated custom editing tool to make analog-style edits. This method sacrifices productivity, introduces the risk of losing design attributes data (also known as metadata), and lacks the ability to readily assess the impact of custom edits on the overall design. Synopsys' IC Compiler and Custom Designer unified solution addresses these challenges and accelerates the product development cycle by providing:

- ▶ Seamless roundtrip custom editing at any stage of the IC Compiler implementation flow to avoid lengthy iterations between the digital and custom environment
- ▶ Comprehensive custom editing capabilities for a broad spectrum of high-precision edits to IC Compiler designs
- ▶ An out-of-the-box solution for easy setup and use to achieve immediate productivity benefits.



Seamless Custom Editing at Any Stage of Implementation

The IC Compiler and Custom Designer unified solution provides a powerful capability to perform seamless roundtrip custom editing of IC Compiler designs throughout the physical implementation flow, including floorplanning, placement, clock tree synthesis, routing and chip finishing while maintaining complete data integrity. This overcomes the limitations of traditional flows employing slow, unwieldy LEF/DEF/GDSII-based scripts that lose important design metadata and lack the ability to reliably manage design changes in both custom and digital place-and-route tools. Some typical applications include:

- ▶ Precise pre-placement of analog macros and adjacent standard cell placement regions
- ▶ Creation of complex supply and ground structures
- ▶ Pre-route of critical nets and special nets such as wide, differential, fully-shielded and matched length/resistance
- ▶ Late-stage editing for final DRC, DFM and ECO needs
- ▶ Addition of manufacture structures such as probe pads, mask markings and seal rings

IC Compiler users can perform custom editing operations using Custom Designer while honoring and maintaining important metadata, such as:

- ▶ Default and Non Default Rules (NDR)
- ▶ Routing grids
- ▶ Standard cell row definitions and placement grid
- ▶ Route keep-outs and blockages
- ▶ Route guides

The metadata can also be added or changed in Custom Designer where it will be seamlessly reflected back in IC Compiler. Preservation of the metadata ensures that custom edits are fully compatible with IC Compiler and allows for the impact of the custom edits, such as timing effects of wire length or width changes, to be assessed in IC Compiler.

Comprehensive Custom Editing Capabilities

IC Compiler users can take advantage of Custom Designer's advanced productivity features, such as:

- ▶ Interactive point-to-point router with auto-tapering for fast NDR- and DRC-correct route creation
- ▶ SmartDRD technology for dynamic DRC visualization, enforcement and error detection with automatic correction
- ▶ Interactive bus creation with automatic bridge and tunnel
- ▶ Automatic via array generation

Additionally, Custom Designer is "metadata-aware" to further improve custom layout productivity for IC Compiler designs. For example, cell instances are automatically snapped to the row sites defined in IC Compiler during a move operation, and the interactive router has an option to conform to the IC Compiler-defined routing grid.

All this comes with push-button access to the same IC Validator physical verification and StarRC™ parasitic extraction tools used by IC Compiler, providing designers with a comprehensive physical implementation solution.

Out-of-the-Box Solution

The IC Compiler and Custom Designer unified solution is easy to set up and works out-of-the-box, allowing immediate productivity enhancements. Setup is minimal, and no predefined libraries, process design kits (PDKs) or technology files are necessary. All required process technology and design information, such as default routing rules, via definitions, layer colors and layer fill patterns, is derived directly from IC Compiler.

The use model is equally straightforward—simply open an IC Compiler design with Custom Designer, make the desired edits and save the design. IC Compiler can then be used to progress to the next step in the place-and-route flow. This can be done multiple times throughout the flow. The unified solution reduces the load on CAD departments and facilitates quick deployment.

Additional Information

The IC Compiler and Custom Designer unified solution consists of 3 products:

- ▶ [IC Compiler](#)
- ▶ [Custom Designer LE](#)
- ▶ [Custom Designer SDL](#)

Visit Synopsys' custom design microsite at <http://www.customdesigner.com> to learn more.



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