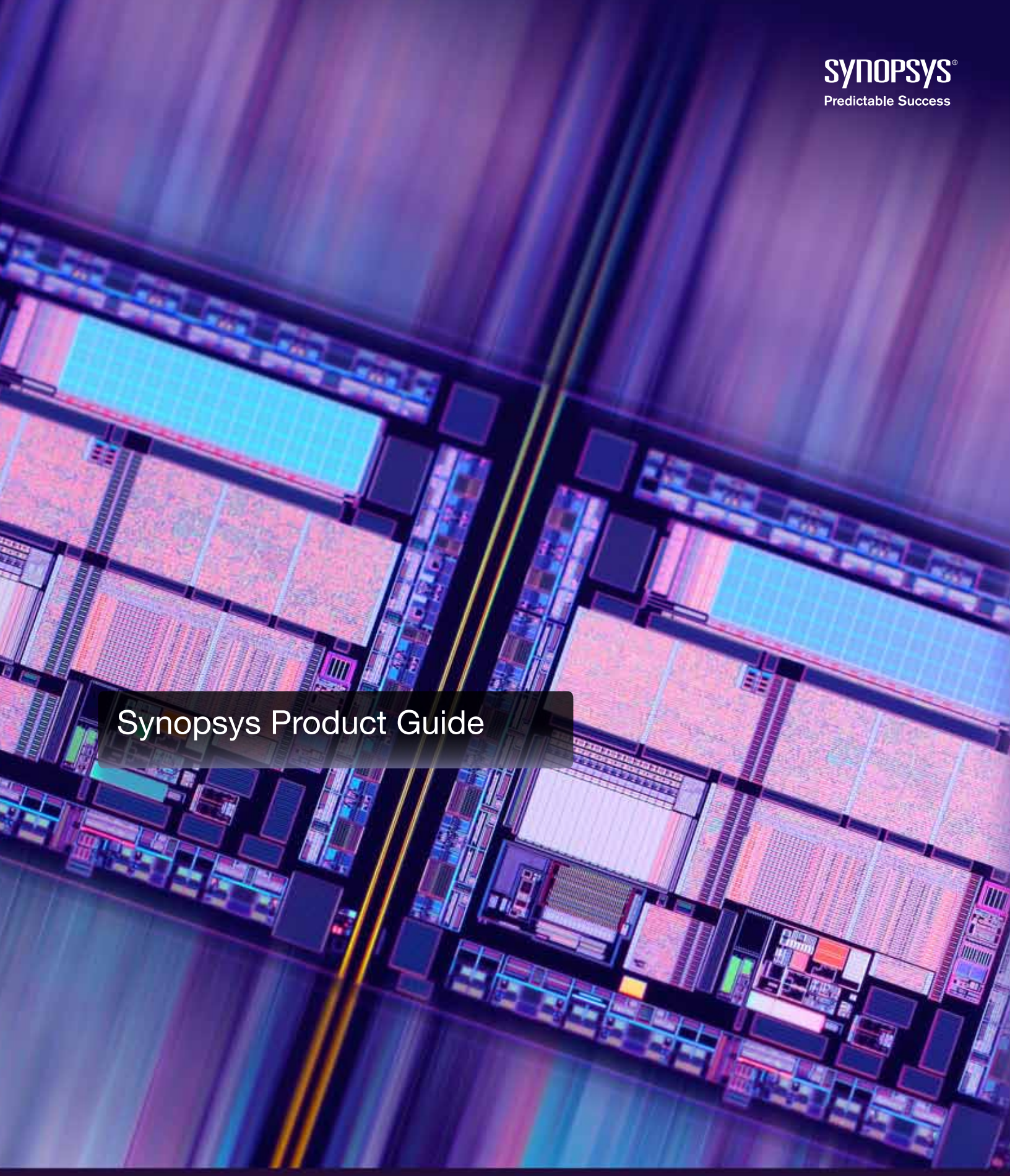
SYNOPSYS®
Predictable Success



Synopsys Product Guide

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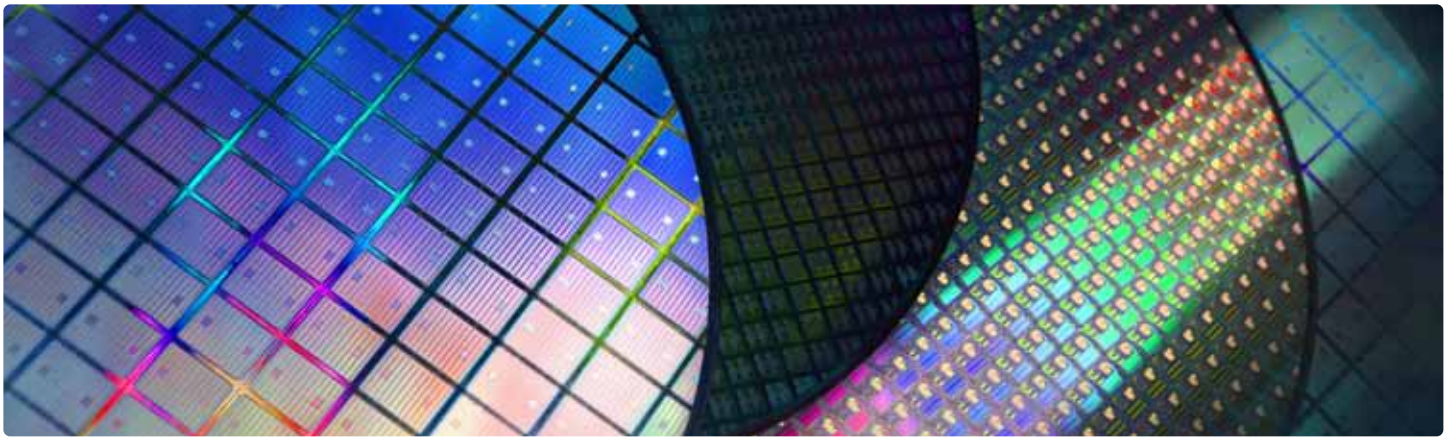
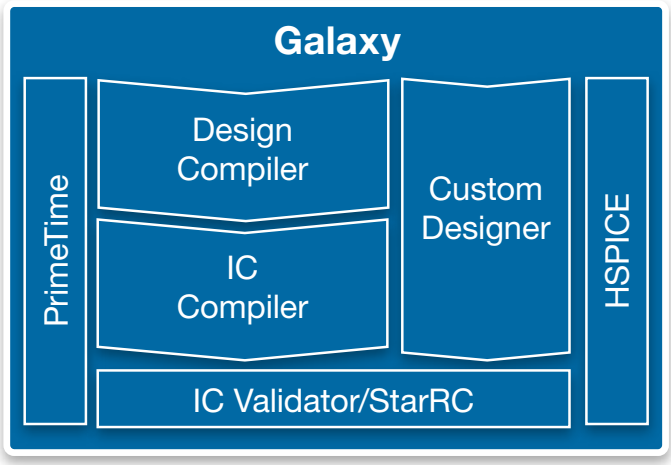
Introduction

This guide provides an overview of Synopsys software, IP and services for semiconductor design and manufacturing. Synopsys' comprehensive, integrated portfolio of system-level, implementation, verification, IP, manufacturing and FPGA solutions helps address the key challenges designers and manufacturers face today, such as power and yield management, system-to-silicon verification and time-to-results. These technology-leading solutions help give Synopsys customers a competitive edge in bringing the best products to market quickly while reducing costs and schedule risk.

Tools



Implementation and Signoff



Custom Implementation

Galaxy Custom Designer™ leverages Synopsys' Galaxy™ Implementation Platform to provide a unified solution for cell-based and custom designs, thereby enhancing SoC design efficiency and productivity. Built from the ground up, Custom Designer was architected for productivity. It is the first-ever custom implementation solution built on an open architecture supporting interoperable process design kits (PDKs) from leading foundries. Custom Designer delivers unmatched productivity with a common use model for simulation, analysis, parasitic extraction and physical verification.

In addition to facilitating innovation with its open architecture, Custom Designer dramatically enhances productivity by seamlessly bridging the gap between the historically disparate worlds of digital and custom design. Custom Designer enables complete data transparency with Synopsys' IC Compiler physical implementation solution, allowing the exchange of vital information during floorplanning, placement, routing and final chip editing to reduce time-consuming design iterations.

Custom Designer SE

Galaxy Custom Designer™ SE is the next-generation choice for

schematic entry, enabling users to meet the challenges of today's fast-moving nanometer designs with little or no learning curve. As with all Custom Designer tools, schematic editing tasks are accomplished with fewer clicks, quicker menu access, and less pop-up menu clutter.

Architected from the ground up with maximum productivity in mind, Custom Designer SE enables ultra-fast schematic editing with on-canvas parameter update and display. SE's real-time connectivity with dynamic net highlighting continuously maintains up-to-date design integrity for faster design with fewer errors and less effort.

Custom Designer leverages the powerful capabilities of Synopsys' Galaxy Implementation Platform to provide a unified solution for custom and digital design teams. Digital teams now have access to a comprehensive analog/mixed-signal (AMS) block authoring flow with an optimized pipeline that eliminates tedious data exchange and leads to faster design cycle time.

Key benefits

- One unified platform for both cell-based and custom content speeds complex chip design and integration tasks
- Supports a complete block-authoring flow with parasitic resimulation for high accuracy results
- Supports Synopsys' CustomSim™, HSPICE®, Custom WaveView and StarRC™ flows for industry signoff physical verification
- On-canvas editing of parameters and nets improves capture time
- Dynamic net highlighting provides fast visual recognition of nets and wires to help eliminate design errors
- Combines testbenches, circuits, simulators, setups, measurements, post simulation processing and analysis into a single environment for fast visualization of results and isolation of problems
- Organizes simulator options and provides easy visualization of all interdependencies and default settings. The simulation options dialog also provides quick help through option-specific tool tips
- Cross-probing and back-annotation between the simulation environment, Custom Designer SE, Custom Designer LE and extracted views lets designers quickly select and display the results that matter for quick analysis directly on the schematic or in Custom WaveView
- Shares all of the Custom Designer tool's advanced infrastructure technology, including the library and hierarchy editors and the job monitor

Custom Designer LE

Custom Designer LE enables ultra-fast layout editing with advanced P-cell support and time-saving layout automation through capabilities like intelligent multipart paths that maintain DRC correctness.

An integral component of the full Custom Designer™ system, LE provides transistor-level layout and editing capabilities in a unified platform for both cell-based and mixed-signal custom content which speeds complex chip design and integration tasks.

Key benefits

- One unified platform for both cell-based and custom content speeds complex chip design and integration tasks
- Supports Synopsys' Hercules™ DRC/LVS and StarRC flows for industry signoff physical verification
- Supports the IPL Alliance's Interoperable PDK libraries for industry-wide design data sharing
- Provides multiple layer purpose pair browsers in a single session when editing designs in multiple libraries

Custom Designer SDL

Custom Designer Schematic Driven Layout Editor (SDL) is an add-on option to the Galaxy Custom Designer™ custom implementation solution and helps boost designer productivity and layout throughput. Architected for productivity, SDL builds on the open foundation of Custom Designer and delivers a complete solution for the layout of today's complex AMS designs. Tightly integrated with Synopsys' industry leading implementation solutions, Custom Designer SDL provides high layout productivity in an easy-to-use environment.

The complex task of implementing today's tough AMS and custom designs requires state-of-the-art tools that are architected for productivity from the ground up. Custom Designer's SDL delivers a high-capacity, high-performance solution for today's complex designs. Custom Designer SDL is fully compliant with all OpenAccess Python-based interoperable process design kits (iPDKs) as well as C++ and Tcl-based PDKs.

Key benefits

- Custom Designer SDL manages and organizes all of the details of correct-by-construction device placement and net connectivity information, enabling everyone from the novice to the advanced designer to be more productive
- Correct-by-construction device placement
- Real-time connectivity through concurrent device and interconnect LVS checking

- High-capacity, high-performance for today's large designs
- Rapid ECO update capability

Cadabra

Library developers are facing increasing challenges at 65 nm and 45 nm nodes, including increasing design rule complexity, time-to-market pressures, library richness, and late design rule changes. Manual layout is becoming increasingly impractical and expensive. Cadabra® offers a fully automated tool for the creation of standard-cell layouts from SPICE netlists, and for migration of existing standard-cell layouts to new design rules or architectures. With easy-to-use graphical interfaces and results that rival hand-crafted techniques, Cadabra is the market leader in automated standard-cell layout.

With advanced manufacturing processes, the number of design rules that must be enforced for each layer is increasing rapidly. Moreover, many of the newer design rules are complex rules that are difficult to visualize, forcing manual layout designers into an iterative flow of layout, design rule checking and correction. Cadabra supports a wide range of advanced rules, including common run and/or width-dependant rules, edge-length rules, and table-based rules.

Key benefits

- Cadabra is key to meeting time-to-market requirements and removing the library from the critical path to access a new process technology
- Optimized for parallel batch processing on a network of computers to allow rapid turnaround time and can interface with many popular job management systems
- Library richness accommodates need for different design goals (high speed, low power, etc)
- Synthesis tools benefit from Cadabra's richer selection of functions and drive strengths
- Cadabra's migration technology allows design rule changes to be incorporated quickly and easily, even in layouts which have been manually optimized

FPGA Implementation

Synplify Pro

The Synplify Pro® FPGA synthesis software is the industry standard for producing high-performing, cost-effective FPGA designs. Its unique Behavior Extracting Synthesis Technology® (B.E.S.T.™) performs optimization first at a high level before synthesizing the RTL code into the specific FPGA architecture. This approach allows for superior optimization across the FPGA, runs fast and supports very large design sizes. The Synplify Pro software supports the latest VHDL and Verilog language constructs including SystemVerilog. Synplify Pro is technology independent allowing quick and easy retargeting between FPGA devices and vendors from a single design project.

Key benefits

- Device-specific mapping technology produces the best quality of results (QoR)
- Industry leading HDL support including SystemVerilog and VHDL 2008
- Targets all popular FPGAs from a single RTL and constraint source
- Automatically optimizes for area reduction (cost) once timing is met
- Fast runtime with consistent results from one pass to the next
- Generates an RTL block diagram from RTL for cross-probing with source code and identifies critical paths
- Automatically extracts and optimizes Finite State Machines (FSMs) based on constraints
- Automatic creation of bubble diagrams for debugging and documenting FSMs
- Extracts and optimizes memory and DSP functions (e.g. MAC) from RTL
- Supports logical equivalency checking flows Eclipse-based IP-XACT block configuration, assembly, and re-use environment
- Tightly integrated with VCS simulator and FPGA vendor place & route tools

Synplify Premier

The Synplify® Premier solution is the industry's ultimate FPGA implementation and debug environment. It provides a comprehensive suite of tools and technologies for advanced FPGA designers as well as for ASIC designers who use single FPGA-based prototypes. The Synplify Premier software is a technology independent solution that addresses the most challenging aspects of FPGA design including timing closure, logic verification, IP usage, ASIC compatibility, DSP implementation, debug, and tight integration with FPGA vendor back-end tools.

The Synplify Premier product offers the most efficient method of design implementation and debug. It provides in-system verification of FPGAs, dramatically accelerates the debug process, and provides a rapid and incremental method for finding elusive design problems.

Key benefits

- Fast Synthesis Mode for quick turnaround
- Integrated RTL debug with advanced triggering
- Prototyping features including DesignWare® support and gated clock conversion
- Fast timing closure through physical synthesis
- Vectorless switching activity (SAIF) generation
- Optional Design Planner for creating floor plans
- Superior Quality of Results (QoR)

Identify

The Identify® RTL Debugger is a software tool that allows users to verify and debug their FPGA design or FPGA-based rapid prototype directly from the source RTL. Identify allows users to probe any signal in the design, specify complex trigger conditions and verify the design at full hardware speed and with real-world stimulus.

The Identify tool allows users to navigate designs graphically and mark signals directly in RTL as probes or sample triggers. After synthesis, results are viewed in the RTL source code or in a waveform. Design iterations are rapidly done using incremental place and route. Identify software is closely integrated with synthesis and routing tools for a seamless development environment.

Key benefits

- Instrument and debug FPGAs directly in RTL source code
- Complex instrumentation including state machine and qualified sampling
- Internal design visibility at full speed
- Fast, incremental debug iterations
- Technology independent—the Identify tool supports devices from Actel, Altera and Xilinx

Identify Pro

The Identify® Pro software, featuring Synopsys' TotalRecall™ technology, provides designers with full visibility into complex FPGA designs and FPGA-based ASIC prototypes enabling them to find bugs at hardware speed and analyze the cause of errors in a familiar simulation environment. Identify Pro software works complementary to other verification methodologies, such as assertion-based verification and simulation, significantly improving the overall productivity.

The Identify Pro software adds advanced triggering and full visibility to FPGA-based prototyping systems, thus making it feasible to detect hard-to-find and sporadic bugs quickly. Upon occurrence of the error condition, Identify Pro software creates the necessary simulation environment including a test bench, so that the bug can be analyzed, fixed and verified in the user's familiar RTL simulation environment. The Identify Pro tool allows users to capture the logic state and the input sequence to the design in hardware just prior to a failure and then simulate and replay the error condition using a standard RTL simulator.

Key benefits

- Full visibility into the design under test
- RTL source code debug
- Automatic testbench generation
- Assertion synthesis and assertion debug
- Technology independent—the Identify Pro debugging and visibility enhancement tool supports devices from Actel, Altera, Lattice and Xilinx

The HAPS High-performance ASIC Prototyping System

The HAPS™ High-performance ASIC Prototyping System is part of the Synopsys Confirma™ Rapid Prototyping Plus Platform. The HAPS products consist of high performance prototyping boards that are ideal for use in system validation and embedded software development.

HAPS is a modular and expandable FPGA-board system consisting of a selection of off-the shelf motherboards and either off-the-shelf or custom designed daughter boards which can be connected in a variety of ways to accommodate and support many design styles and requirements. The motherboards vary in size from one-FPGA to multiple FPGA interconnected devices. The connections between FPGAs in the multi-FPGA motherboards can, if needed, be expanded by adding standard interconnect boards. These daughter boards connect two or more HapsTrak connectors, thus adding additional wires between the FPGAs. This unique modularity of the HAPS prototyping system enables the reuse of the same motherboards for several projects or configurations, simply by adding or replacing daughter boards or subsystems.

Certify

The Certify® software is the leading multi-FPGA implementation and partitioning tool for ASIC designers who use FPGA-based rapid prototypes to verify their designs. Certify provides a quick and productive method for partitioning large ASIC designs onto multi-FPGA rapid prototyping boards and includes powerful features that make it easy to adapt to existing device flows, speeding the verification process and helping to ease time-to-market challenges. The Certify software includes the industry standard Synplify Premier synthesis engine and supports most leading FPGA devices.

CHIPit

The CHIPit® rapid prototyping systems feature a programmable interconnect architecture for more automated design implementation and enabling use modes and debug capabilities. Based on the latest FPGA technologies and complemented by an integrated set of tools, including comprehensive debug capabilities, the modular CHIPit systems can be used in diverse verification modes giving design engineers unprecedented productivity and flexibility to verify chip implementation and system functionality, thereby significantly reducing overall verification time.

Synphony HLS

Synphony HLS is a language and model-based high level synthesis (HLS) technology that provides an efficient path from algorithm concept to silicon. Designers can construct high level algorithm models from math-languages and IP model libraries, and then use the Synphony HLS engine to synthesize optimized RTL implementations for ASICs and FPGAs, architectural exploration and rapid prototyping. In addition, Synphony HLS also generates high-performance C-models for system validation and early software development in virtual platforms.

Physical Implementation

As part of the Galaxy™ Implementation Platform, IC Compiler provides an industry-leading and production-proven solution. IC Compiler is a comprehensive design planning, place-and-route system that includes extended physical synthesis, signoff-driven closure with PrimeTime® and StarRC™, advanced yield optimization, physical power, physical DFT and complete design planning for both flat and hierarchical design.

IC Compiler

IC Compiler is an integral part of the Synopsys Galaxy Implementation Platform that delivers a complete design solution, including synthesis, physical implementation, low power design, and design for manufacturability (DFM). IC Compiler is a single, convergent, chip-level physical implementation tool that includes flat and hierarchical design planning, feasibility, placement and optimization, clock tree synthesis, routing, design for manufacturing (DFM), and low-power capabilities that enable designers to implement today's high-performance, complex designs. Widely adopted and recognized as the industry standard for physical implementation, IC Compiler provides best-in-class QoR, strong signoff correlation, and powerful DFM capabilities.

Key benefits

- High throughput for designs in mainstream silicon technologies
- High performance for advanced silicon technologies
- Complete netlist-to-GDSII solution for best QoR, TTR and predictability
- Production proven at 45/40 nm and 32/28 nm technology nodes
- Faster time to results (TTR) enabled by multicore support throughout the flow
- Reduced cost of design with concurrent design planning and implementation feasibility capabilities
- Comprehensive optimization capabilities meet timing, area, power, signal integrity (SI), routability and yield objectives
- Handles variation affects with complete multi-corner, multi-mode (MCMM) support throughout the place and route (P&R) flow, clock mesh and advanced on-chip analysis (AOCV) capability
- Advanced rule support and better DFM QoR with Zroute technology
- Shares common infrastructure and technologies with PrimeTime, such as Arnoldi, on-chip variations (OCV), clock reconvergence pessimism removal (CRPR), composite current source (CCS), common cell delay calculation and Synopsys design constraints (SDC) to ensure tight correlation and faster design convergence
- Complete low power support throughout the flow, including multi-voltage, MTCMOS support and dynamic and leakage power optimization
- Faster design closure using "companion links" with implementation and signoff tools such as Design Compiler® Graphical, PrimeTime®-SI, StarRC, IC Validator, PrimeRail and PrimeYield LCC

Physical Verification

Physical Verification, as part of Synopsys' Galaxy Implementation Platform, provides comprehensive, production-proven solutions for design rule checking (DRC), layout verification (LVS), and practical DFM applications, such as lithography compliance checking (LCC). The latest signoff DRC/LVS offering, IC Validator, is architected for In-Design Physical Verification within IC Compiler.

IC Validator

Architected to work closely with IC Compiler, IC Validator is built on shared data models and processing engines, resulting in an integrated In-Design Physical Verification flow that delivers signoff-level accuracy coupled with faster overall total physical verification time. This is done via In-Design Physical Verification, stream-out reduction, incremental processing, and automatic error detection and correction. In-Design integration also enables fast, timing aware implementation of DFM such as metal fill. IC Validator delivers near-linear scalability for efficient utilization of available hardware, superior ease-of-use for the physical designer, and high programmability for easier runset development.

IC Validator is fully qualified for DRC/LVS signoff at the current 45 nm and 40 nm process nodes as well as the emerging 32 nm and 28 nm nodes at major integrated device manufacturers (IDMs) and foundries.

Key benefits

- Fast overall physical verification turnaround time with in-design physical verification
- Fast runtime with near-linear scalability
- Signoff accuracy and high productivity with Layout-vs-Schematic (LVS) integration with Star RC
- Ease of debug with VUE GUI
- Custom Designer integration
- Production proven and foundry-qualified at 45 nm and 32 nm
- High programmability with PXL language

PrimeYield LCC

PrimeYield LCC is a foundry-qualified lithography-checking tool for 65 nm and smaller technology nodes. Built on production-proven technology and manufacturing models used by the leading foundries and IDMs, PrimeYield accuracy allows designers to focus on real potential escapes and avoid extra effort on false positives.

Key benefits

- Accurate analysis based on production-proven manufacturing data
- High productivity with automated find-and-fix guidance to IC Compiler
- Ease of debug with VUE GUI

RTL Synthesis and Test

Design Compiler® in the Galaxy™ Implementation Platform maximizes your productivity with its suite of RTL synthesis and test solutions. The premier synthesis product, DC Ultra, lets you accurately predict post-layout timing, area and power during RTL synthesis, to significantly reduce costly and time-consuming design iterations. Design Compiler Graphical enables RTL designers to predict, visualize and alleviate wire routing congestion and perform floorplan prior to physical implementation. Additionally, it produces "physical guidance" to the IC Compiler place-and-route solution for tighter correlation and faster placement runtimes. The Design Compiler family also includes: the award-winning Galaxy Test solution for the fastest, most cost-effective path to high-quality manufacturing tests and working silicon; Power Compiler™, for power synthesis and optimization; the Formality® equivalence checker; and the DesignWare® library with its unequalled variety of synthesizable IP. These best-in-class, production-proven solutions are integrated to achieve the industry's fastest and most predictable RTL-to-GDSII flow.

Design Compiler 2010

Continuing the trend of delivering innovative synthesis technology, Synopsys offers Design Compiler 2010 that provides a twofold speedup of the synthesis and physical implementation flow. As geometries shrink to 65 nm and smaller process technologies, design complexities increase multifold making it extremely difficult for designers to complete designs on schedule. The nanometer effects such as coupling capacitances between parallel interconnects have much higher impact on interconnect delays and need to be considered during synthesis for predictable design implementation. Moreover, floorplan issues, such as routing congestion due to macro placement, need to be fixed early in the design cycle to avoid iterations. Designers need an RTL synthesis solution that improves schedule predictability by producing a better starting point to physical implementation and avoids costly iterations between synthesis and place and route.

Key benefits

- Better starting point for physical implementation
  - 5% Correlation to layout
  - 1.5X faster placement runtime
  - Push-button floorplan exploration
- 2X faster runtime on quad-core compute servers

Design Compiler Ultra

Design Compiler® Ultra (DC Ultra) is the best-in-class, production RTL synthesis solution enabling users to meet today's design challenges such as fastest timing, smallest area, lowest power consumption and highest test coverage in the shortest design cycle time. DC Ultra achieves this by concurrently applying its unique algorithms to optimize for timing, area, power and test.

DC Ultra includes innovative Topographical technology that enables a predictable flow resulting in faster time to results by eliminating costly iterations between synthesis and layout. Topographical technology accurately predicts post-layout results such as timing, power and area in synthesis to help designers reduce costly iterations between synthesis and physical implementation.

Key benefits

- Delivers best Quality of Results (QoR) in terms of area, timing, power and test
- Results correlate to physical implementation
- Removes timing bottlenecks by creating fast critical paths
- Offers more flexibility for users to control optimization on specific areas of designs
- Enables higher efficiency with integrated static timing analysis, test synthesis and power synthesis
- Support for multi voltage and multi supply
- 2X faster runtime on quad-core compute servers

Design Compiler Graphical

Design Compiler® Graphical is designed to increase designer productivity for both synthesis and place and route through creation of a better starting point for physical implementation and eliminating costly iterations between synthesis and place and route. It extends DC Ultra™ topographical technology to predict circuit congestion "hot spots" early in the design flow, provides designers with visualization of congested circuit regions and performs specialized synthesis optimizations to minimize congestion in these areas. This enables RTL designers to avoid wire-routing congestion problems that occur during detailed routing. Additionally, it provides RTL designers access to IC Compiler's design planning capabilities from within the synthesis environment. With the push of a button, they can perform what-if floorplan exploration to identify and fix floorplan issues such as timing issues due to macro locations and achieve an optimal floorplan efficiently.

Design Compiler Graphical applies additional physical optimization techniques and considers the effects of smaller geometries such as coupling capacitances for accurate delay modeling. It produces physical guidance to IC Compiler place and- route solution tightening timing and area correlation to 5% while speeding-up IC Compiler placement by 1.5X. The physical guidance passed to IC Compiler streamlines the flow for a faster, predictable and convergent path from RTL to GDSII. In addition, Design Compiler Graphical includes a scalable multicore infrastructure designed to deliver significant runtime speed-up on multicore compute servers yielding 2X faster runtime on four cores.

Key benefits

- Improved schedule predictability with accurate congestion prediction in synthesis
- Reduced routing congestion with specialized congestion-driven optimizations
- Early detection and debugging of layout issues using physical visualization for faster convergence
- Push-button floorplan exploration within the synthesis environment
- Physical guidance to IC Compiler delivering 5% correlation to layout and 1.5X placement runtime
- Concurrent multi-corner, multi-mode (MCMM) synthesis
- Reduces iterations between synthesis and place and route
- Early detection and fixing of design issues otherwise handled late in the design process
- Superior starting point for place and route for faster physical implementation

Power Compiler

Reducing power consumption is required in today's semiconductor designs. Silicon technology advances have made it possible to pack millions of transistors switching at high clock speeds on a single chip. While these advances bring unprecedented performance to electronic products, they pose difficult power dissipation and distribution problems. These problems must be addressed, because consumers demand longer battery life in addition to lower cost in computers, battery-operated systems, medical devices, telecommunications equipment and many high-volume consumer products.

Power Compiler™ automatically minimizes power consumption at the RTL and gate level. Power Compiler automatically applies several different synthesis techniques such as automatic clock gating and multi-voltage threshold library optimization to reduce power consumption and achieve optimal leakage. Driven by design constraints, it performs concurrent optimization for timing, power and area. With power intent defined by the industry standard IEEE 1801-2009 Unified Power Format (UPF) specification, it automatically inserts power management cells such as isolation, level-shifter, retention registers, power gates and always-on cells as needed. Power Compiler is seamlessly integrated with the synthesis design flow and shares the same GUI, commands, constraints and libraries with the Design Compiler and IC Compiler tools.

Key benefits

- Supports advanced low power techniques such as multiple voltage domain synthesis and automated power management cell insertion
- Provides accurate timing and power analysis correlation (within 10%) of actual place and route results early in the synthesis design cycle when used in conjunction with DC Ultra
- Automated clock gate balancing and re-configuration optimization for hierarchical (global), power-driven, and multi-stage designs. Supports multi-threshold libraries for optimal leakage
- Robust power model estimates and controls: switching (capacitive) power; internal (short circuit) power, and leakage (static) power

DFTMAX

DFTMAX™ compression is a comprehensive test compression solution that addresses the cost challenges of testing complex designs, particularly when fabricated with small process technologies. These deep-submicron (DSM) designs can have subtle manufacturing defects that are only detected by applying DSM tests, such as at-speed and bridging tests, in addition to stuck-at tests. The extra patterns needed to achieve high test quality for these designs can increase both the test time and the test data, resulting in higher test costs.

DFTMAX compression reduces these costs by delivering push-button 10-100X test data and test time compression with very low silicon area overhead. Seamlessly enabling compression in TetraMAX® ATPG, and encapsulated in Synopsys' Galaxy™ Design Platform, DFTMAX compression achieves predictable results with virtually zero impact on timing.

Key benefits

- Lowers test costs
- Provides high defect coverage
- As easy-to-use as standard scan
- Avoids any impact on design timing
- Leverages physical design for area optimization
- Minimizes area impact
- Minimizes required number of test pins
- Preserves low-power design intent
- Minimizes power consumption during test

TetraMAX ATPG

TetraMAX® ATPG automatically generates high quality manufacturing test patterns. It's the only ATPG solution optimized for a wide range of test methodologies and integrated with Synopsys' patented DFTMAX™ compression the leading test synthesis tool. The unparalleled ease-of-use and high performance provided by TetraMAX ATPG allows RTL designers to quickly create efficient, compact tests for even the most complex designs.

Key benefits

- Increases product quality with power-aware test patterns for high defect detection
- Reduces testing costs through the use of advanced pattern compaction techniques
- Increases designer productivity by leveraging integration with Synopsys DFTMAX compression
- Creates tests for complex and multi-million gate designs

Formality

The size and complexity of today's designs, coupled with the challenges of meeting timing, area, power and schedule, requires that the newest, most advanced synthesis optimizations be fully verifiable. Formality® is an equivalence-checking (EC) solution that uses formal, static techniques to determine if two versions of a design are functionally equivalent. Formality supports all of the out-of-the- box DC Ultra™ optimizations and therefore provides highest quality of results that are fully verifiable. It supports verification of power-up and power-down states, multi-voltage, multi-supply and clock gated designs.

Formality's easy-to-use, flow-based graphical user interface and auto-setup mode helps even new users successfully complete verification in the shortest possible time.

Key benefits

- Perfect companion to DC Ultra – supports all DC Ultra default optimizations
- Intuitive flow-based graphical user interface
- Verifies low-power designs including power-up and power-down states
- Auto setup mode reduces "false failures" caused by incorrect or missing setup information
- Built-in distributed verification boosts performance
- Automated guidance boosts completion with DC Ultra
- Verifies full-custom and memory designs with ESP option

Signoff

Unleashing the performance potential of advanced silicon process technology without the risk of design failure is one of the single biggest design closure challenges facing designers. Synopsys brings a broad integrated portfolio of state-of-the art design analysis and signoff technology all based on the golden

signoff foundation customers have come to trust. The Galaxy™ signoff solutions deliver all the ingredients necessary from library generation with composite current source (CCS) modeling to statistical timing analysis, advanced signal integrity and IR-drop based analysis and signoff. Combining Galaxy signoff with IC Compiler physical implementation solutions' tight correlation and ECO integration allows designers to confidently unleash the full performance potential with the fastest design closure.

PrimeTime

The Synopsys PrimeTime® suite, provides a single, golden, trusted signoff solution for timing, signal integrity, power and variation-aware analysis. It delivers HSPICE® accurate signoff analysis that helps pinpoint problems prior to tapeout thereby reducing risk, ensuring design integrity, and lowering the cost of design. This industry gold-standard improves your team's productivity by delivering fast turnaround to shave precious time from development schedules for large and small designs while ensuring first-pass silicon success through greater predictability and the highest accuracy.

Key benefits

- HSPICE-accurate results minimize over-design
- Integrated design environment improves productivity
- Fast turn-around time speeds analysis and signoff
- High capacity approach reduces hardware costs
- Complete solution ensures comprehensive signoff

Galaxy Constraint Analyzer

Galaxy™ Constraint Analyzer improves designer productivity through look-ahead timing constraint analysis and debug technology tuned for the Synopsys Galaxy Implementation Platform. Early feedback on constraint quality leads to more efficient runtimes and better quality of results in Synopsys' Design Compiler synthesis and IC Compiler physical implementation tools.

Galaxy Constraint Analyzer provides an intuitive interactive environment for designers to quickly assess the correctness and consistency of timing constraints, helping eliminate trial-and-error iterations during implementation and thereby resulting in more predictable schedules and reduced design cost.

Key benefits

- Powerful timing rule checks which cover pre- and post-layout timing conditions
- Supports Galaxy-specific rule checks to help users create constraints which maximize efficiency in Design Compiler, IC Compiler and PrimeTime
- Best-in-class debug solution allows users to debug reported violations in real time using the interactive graphical user interface
- Debugging guidance and constraint fixing recommendations
- Fast runtimes enabling interactive analysis and debug sessions
- Common user interface with the Galaxy Implementation Platform tool suite.
- Intuitive interface with user-selectable levels of reporting

NanoTime

Synopsys' NanoTime® tool is the next-generation transistor-level static timing analysis solution that addresses the emerging challenges in SI analysis associated with custom designs. NanoTime offers concurrent timing and SI analysis, accuracy within five percent of HSPICE®, and the performance required to analyze complex transistor circuits overnight. Its seamless integration with Synopsys' PrimeTime® product enables full-chip analysis of designs that includes both gate- and transistor-level blocks. NanoTime is a key component of the Synopsys custom design verification solution that includes NanoSim®, HSIM and HSPICE for circuit simulation and ESP-CV for symbolic simulation.

Key benefits

- Concurrent timing and SI analysis provides higher predictability and better productivity over existing solutions
- Delivers accuracy within 5% of HSPICE
- Ease of use features improves productivity
- New algorithms result in a five-fold increase in performance over existing solution without sacrificing accuracy
- Industry-standard support, Liberty, SDC, SPF, SPEF

PrimeRail

PrimeRail is the rail analysis technology foundation for IC Compiler In-Design Rail Analysis. Invoked directly from IC Compiler, In-Design Rail Analysis utilizes embedded PrimeRail analysis and fixing guidance technology to enable designers to easily perform power network verification throughout physical implementation. By identifying and fixing voltage-drop and electromigration issues earlier in the flow, designers can eliminate costly iterations late in the design process. Built on industry gold standard PrimeTime SI and StarRC signoff technologies, PrimeRail offers high-accuracy, full-chip SoC static and dynamic rail analysis to accelerate design closure.

Key benefits

- Integrated IC Compiler In-Design Rail Analysis environment
- Push button setup and data integrity checking to streamline flow

- Milkyway™ database integration to eliminate costly tool input and outputs
- Integrated display environment overlaying maps directly with layout
- Integrated error browser with detailed reporting and fixing guidance to rapidly pin-point, isolate and fix potential issues
- Ability to run, analyze, fix and debug throughout the IC Compiler flow from design planning, pre-layout and post-layout to chip finishing
- Comprehensive dynamic and static rail analysis
- Multi-million instances-per-hour performance and within 10% HSPICE accuracy

StarRC

The StarRC™ solution is the EDA industry's gold standard for parasitic extraction. A key component of Synopsys Galaxy™ Implementation Platform, it provides a silicon-accurate and high-performance extraction solution for SoC, custom digital, analog/mixed-signal (AMS) and memory IC designs. StarRC offers modeling of advanced physical effects needed for leading-edge process technologies, including 28 nm. Its seamless integration with industry standard digital and custom implementation systems, timing, signal integrity, power, physical verification and circuit simulation flows delivers unmatched ease-of-use and productivity to speed design closure and signoff verification.

Key benefits

- Best-in-class multicore performance and delivering up to 8X speed up with 16 cores
- Embedded fast field solver (FFS) technology ensuring high-accuracy extraction for critical IP within the single StarRC environment
- Optimized links with Synopsys CustomSim™ enabling up to 10X speed up in simulation
- Integration with Synopsys Galaxy Custom Designer™ and Cadence® Virtuoso® custom design

Liberty NCX

The Liberty™ NCX solution is a complete library delivery system specially architected for current-source models that features an optimized, single-pass composite current source (CCS) library generation flow that performs simultaneous characterization and model accuracy verification. Liberty NCX supports all the latest open-source Liberty modeling innovations approved by the Liberty Technical Advisory Board (TAB).

Key benefits

- Intuitive, easy-to-use interface
- High performance via adaptive, fine-grain simulation job parallelization and HSPICE client-server support
- Variation-aware (statistical) characterization
- Automated index point selection
- Native base-curve compaction support enabling smallest library file size

Manufacturing

Synopsys provides industry-proven EDA solutions to meet the demands of today's advanced IC manufacturing processes while setting the standard in platform flexibility to enable innovative and custom solutions for next generation technology nodes. Synopsys' comprehensive Mask Synthesis, Mask Data Prep, TCAD and Yield Management tools provide leading-edge performance, accuracy, quality and cost of ownership for all your production and development needs.

Mask Synthesis

Proteus

Proteus OPC provides industry-proven scalability and lowest cost of ownership. Significant performance gains have been realized with the introduction of the Proteus Pipeline Technology in 2008. Since then, pipelining has been adopted by leading-edge customers and is ready for full deployment along with Proteus' pipelined advance resolution enhancement techniques (RET) and next-generation verification:

Key benefits

- Proteus MBAF—Inverse-mask lithography and intensity-based model-based AF placement, clean-up, and printability fixing
- Proteus DPT—Double-patterning decomposition with its unique cost-based solver and built-in design and MRC compliance
- Proteus LRC—Proteus' next-generation lithography rule checker to address the unique complexity for 45 nm and beyond
- Sentaurus Lithography—Predictive simulation for development and optimization of immersion, double-patterning, extreme ultraviolet (EUV), and e-beam lithography processes

Mask Data Preparation

CATS

CATS® is the industry leading solution for converting design data into machine readable data formats for e-beam and laser machines used for photomask manufacturing, inspection and metrology. CATS has installations in virtually every photomask manufacturing facility worldwide, and is the de facto standard for mask manufacturing, inspection, metrology, and direct-write-on-wafer.

CATS delivers the fastest mask throughput times by implementing innovative techniques in optical proximity correction-mask data preparation (OPC-MDP) pipelining, scalability over hundreds of cores and superior quality of fracture that leads to faster mask write times.

Key benefits

- Fast mask throughput for advanced technology nodes
- Superior quality of fracture
- Comprehensive solution for mask write, inspection and metrology
- High-speed, intuitive graphical interface
- Advanced manufacturing rule checks and comprehensive Boolean operations

Manufacturing Yield Management

Yield Explorer

Yield Explorer is a design-centric yield management system uniquely capable of resolving yield issues caused by design-process-test interactions in nanometer silicon technology nodes. A complement to the Synopsys TetraMAX® diagnostics solution, Yield Explorer is a timely solution to the complex challenges faced by today's product engineering teams. With the widest possible range of data at their disposal, users achieve unsurpassed clarity in root cause analysis when faced with systematic yield limiters. Yield Explorer enables correlating the output from ATE tests, wafer parametric data, physical design attributes, design rule check (DRC) results and static timing distribution across the chip and other yield relevant data in a single application for the first time.

Key benefits

- Very high accuracy in locating systematic yield limiters within a failing chip
  - >90% accuracy with volume diagnostics methodology
- An order of magnitude acceleration of analysis speed in most complex of the use cases
  - 10X faster volume diagnostics analysis over thousands of failing dies
- One-stop solution for comprehensive yield improvement at nanometer nodes
  - Single data bank and analysis engine for design, fab and test data

System-Level Design

Synopsys provides a comprehensive portfolio of system-level products that bridge the gap from system design to implementation. These products include: Innovator for building virtual prototype solutions and enabling pre-silicon software development; Platform Architect for SystemC platform capture and architecture analysis; Processor Designer for accelerating the design of custom processors and programmable accelerators; SPW/System Studio for the fastest path from innovation to implementation of digital signal processing systems; Synphony HLS enabling high level synthesis for FPGAs and ASICs; and the Saber platform for designing and verifying Mechatronic Systems and wire harnesses. The tools are complemented by libraries that contain an extensive set of models to accelerate development. The Synopsys system-level products improve the productivity of the entire project team by addressing the challenges at the front end of both hardware and software development flows.

Processor Development

As companies are looking to improve their competitive advantage, the need for programmable hardware accelerators, ASIPs and custom processors is growing rapidly. They provide the solution to performance and flexibility challenges system designers are facing today. Processor Designer offers exactly this: design flexibility without compromises.

Processor Designer

Synopsys Processor Designer dramatically accelerates the design of both application-specific processors and configurable accelerators through automated software development tools, RTL and instruction set simulator generation from a single, high-level specification. These application-specific processors and configurable accelerators are increasingly essential to convergent system-on-chip (SoC) functionality. Processor Designer is used

to develop a wide range of processor architectures, including architectures with DSP-specific and RISC-specific features as well as SIMD and very long instruction word (VLIW) processors.

Processor Designer's generated software development environment enables the commencement of application software development prior to silicon availability, thus eradicating a common bottleneck in embedded system development.

Key benefits

- Integrated design environment for unified application-specific processor, programmable accelerator design and software development tool generation
- Slashes application-specific processor and programmable accelerator hardware design time by months
- Eliminates months of engineer-effort for software tool development
- Ensures compatibility of instruction set simulator (ISS), software development tools and RTL implementation
- Software development environment enables application software development prior to silicon availability
- Non-intrusive multi-core debugging

Virtual Prototypes

Virtual prototypes are fast simulated models of an electronic system and are used for software development, integration and test, and verification. They can be available months before first silicon is available. Their packaging and distribution enables concurrent hardware and software engineering within and across companies. Virtual Prototypes provide significant benefit because the dependency on physical hardware availability is removed. They complement traditional software development tools, with debug and analysis tools that provide unmatched visibility and controllability into the behavior of the electronic system, both hardware and software. Synopsys provide a complete solution including models, tools, methodologies and services for the creation and use of virtual prototypes.

Innovator

Synopsys Innovator is a SystemC™-based integrated development environment (IDE) for virtual prototype developers to efficiently integrate, analyze and verify transaction-level models (TLMs). In addition to re-using any existing IEEE 1666 SystemC models with arbitrary interfaces, Innovator enables the authoring of Open SystemC Initiative's (OSCI) SystemC TLM-2.0 compatible models.

Once a virtual prototype is assembled and verified with Innovator, it can be delivered to programmers as a standalone, run-time executable, seamlessly fitting into software developers' work flows. Innovator provides open interfaces for software debuggers and software development tool chains. In combination with the Synopsys DesignWare® System-Level Library of standards-based TLMs, Synopsys Innovator significantly increases productivity for creating, assembling and deploying virtual prototypes. Innovator supports SystemC loosely timed (LT) modeling for pre-silicon software development and SystemC approximately timed (AT) modeling for architecture analysis as well as links to RTL verification.

Key benefits

- Arbitrary IEEE 1666 SystemC and TLM-2.0 Import
- SystemC model import
- TLM-2.0 model authoring
- Intuitive handling of hardware concurrency via graphical representation of C++ and SystemC models
- Peripheral creation
- Intuitive design capture
- SystemC IEEE 1666 simulation engine
- Connectivity browser, greatly simplifying design navigation
- SystemC model availability with the DesignWare System-Level Library
- Advanced simulation, debug and analysis for software development
- Compatibility with standard software development tools, allowing software developers to remain in familiar development environments
- Scripting, including command handling on a per-instance basis, the ability to define multiple parameter sets, and regression testing
- Non-intrusive multi-core debugging

Platform Architect

Synopsys Platform Architect provides a common design and use environment for system-level design activities using virtual prototypes such as architecture design, system verification, software development, integration and test. Platform Architect leverages modeling standards such as SystemC™/TLM 2.0 to enable users to create a virtual prototype at multiple levels of abstraction (cycle accurate, approximately and loosely timed, untimed). Virtual prototypes enable IP, semiconductor and system companies to define, develop and deploy electronic systems faster and increase developer's productivity.

Platform Architect includes a complete integrated development environment for SystemC-based virtual prototyping. The SystemC Wizard enables users to automatically create peripheral models.

The assembly can be performed through a graphical tool or scripting. The created virtual prototype can be validated using a native SystemC simulator and a powerful Eclipse-based and SystemC aware, intuitive debugging tool. The result is a virtual prototype created in a matter of days rather than months.

Platform Architect is completed by a rich library of processor, bus, and peripheral models. Processor models include cycle-accurate and instruction-accurate models from leading processor vendors. Third-party processor models can be integrated through a documented API. AMBA®, AXI and PL301 interconnects, as well as ARM Primecell and DesignWare® System Level Library, are examples of the models available. In addition, users can integrate existing models created using C or C++, uplift RTL and interface with third-party simulators such as an HDL simulator or Simulink.

Platform Architect enables software-driven SoC architecture design using traffic generation such as generic file reader bus masters and virtual processing used with application task mapping as well as cycle-accurate to loosely-timed processor models running actual software. For architectural analysis, Platform Architect provides views to analyze cycle-accurate performance, study throughput and bottlenecks, look at bus switching and cache usage to reduce power and optimize bus & memory architecture. For functional analysis, Platform Architect provides views to look at system response and task scheduling, analyze processor loading to drive partitioning, profile software for optimization and to cross-correlate different views to extract powerful information. Analysis views can be configured at run-time using SystemC Explorer (a Platform Architect feature), enabling the user to decide on the data that is captured. The visualization environment allows the user to see the default graphical views dynamically during simulation or during post-processing to identify bottlenecks in the design. Views can be re-configured as required and data from multiple simulations can be grouped together for easy comparison of candidate architectures.

Platform Architect enables developers to generate a virtual prototype as a self contained, distributable and protected package for software developers. The self-contained package can be easily distributed in advance of physical hardware availability--even pre-RTL. The virtual prototypes include the simulation of the electronic system as well as powerful software development tools that complement the use of traditional source code software debuggers. The Virtual Platform Analyzer enables developers to do platform-level debugging by setting break points on any part of the model registers and pins. The tool is fully customizable through a powerful scripting automation interface enabling developers to be more productive and insert virtual prototypes in their development, integration and test flows. The software analysis provides developers with the ability to quickly understand the behavior of the software with capabilities such as function tracing, cache hit and miss and code coverage. The software tools are OS aware. All debugging and analysis tools (including third parties) are synchronized, thus making the debugging of homogenous or heterogeneous multicore systems more efficient. Using Virtual Prototypes for software development enables developers to debug and fix problems in a matter of hours rather than days.

Key benefits

- Common, rapid capture and configuration of hierarchical SoC and full electronic systems for architecture design, system verification and software development
- Native SystemC/TLM-2.0 modeling environment including SystemC aware platform debugger
- Automated creation of highly-reusable, user-defined SystemC peripheral components and unit tests as well as automated integration of RTL blocks into the TLM system
- Standards-based SystemC TLM modeling guidelines and examples using SCML and TLM-2.0
- Rich library of processor, interconnect and peripheral models
- Superior architecture and performance analysis for SystemC
- Rapid exploration of complex interconnect and memory architectures
- High-speed simulation for software development
- Platform-level software debugging and hardware/software analysis and synchronized integration with third-party software debuggers
- Fully scriptable and customizable tools to meet specific needs

CoMET/METeor/Metrix

Synopsys CoMET® is a system engineering tool that enables the creation of a software simulation-based virtual prototype of a system-on-a-chip. The virtual prototype is used to enable concurrent design of hardware and software. Virtual prototypes are assembled from a basic set of CoMET/METeor® models as well as models a user can create using the Peripheral Device Builder (PDB). With CoMET you can design, simulate, analyze, and optimize complex embedded systems and quantitatively evaluate performance while running real software. CoMET enables high-speed, timing-accurate virtual prototype modeling and is well suited for applications such as automotive control.

METeor is an interactive, real-time software development environment for embedded systems and system-on-chip (SoC).

With METeor you can use the virtual prototype created with CoMET to develop, simulate, debug and optimize embedded software many months before the hardware becomes available.

Metrix™ provides a monitoring and measurement solution to the virtual prototype user. Users can stream, process, present, and analyze hardware/software interactions and develop custom views to analyze design-specific behavior.

Using Synopsys CoMET/METeor, users can rapidly explore 100s of parameters and optimize a design in a fraction of the time, hand off virtual prototypes to software developers who do not have to wait for hardware before beginning software development, thus reducing software development time.

Key benefits

- Rich library of peripheral models including memories, timers, and interrupt controllers and VPM processor models. Support for DesignWare® System-Level Library
- Automated creation of new peripheral models using Peripheral Device Builder (PDB)
- Support for customer created C, C++ and System C™/TLM models
- Rapid and configurable prototype assembly environment built on Eclipse
- High-speed timing accurate simulation
- Hardware and software concurrent debugging
- Co-Simulation with HDL simulator for RTL verification in the context of the system-level simulation

DesignWare System-Level Library

The Synopsys DesignWare® System-Level Library provides product development teams with a comprehensive set of standards-based, tool-independent TLMs that serve as the building blocks of virtual prototypes. Virtual prototypes are fully functional software models of complete embedded systems, enabling pre-silicon software development and software-driven system validation. The ability to parallelize the hardware and software development effort through virtual prototypes significantly reduces the product design cycle and speeds time to market.

The OSCI TLM-2.0-compliant models in the DesignWare System-Level Library are written in SystemC™ to function with any IEEE 1666-compliant SystemC simulator. Mirroring the productivity gains realized by IP reuse in the implementation phase, the System-Level Library accelerates the development of virtual prototypes by providing pre-defined abstract models of hardware components in wireless, multimedia, networking and automotive application domains.

Key benefits

Production-proven transaction-level models (TLM's), including:

- High-performance processor models
- Synopsys DesignWare Interconnect IP models
- Synopsys DesignWare AMBA® component models
- ARM® PrimeCell models
- Infrastructure models
- Pre-assembled prototypes assembled from transaction-level models that serve both as demo vehicles as well as starting points for new virtual prototype development
- Written in SystemC to run with any IEEE 1666-compliant SystemC simulator
- TLM-2.0 compliant
- Model Authoring Kits to accelerate the development of customer-specific models by providing software building blocks

System-Level Modeling Services

See Services section page 44 for more information.

Digital Signal Processing

Algorithm design is an essential element of digital signal processing (DSP) applications such as wireless telephony, multimedia codecs, DSL and cable modems. To a large degree, the algorithms that users develop have a significant impact on the performance and functionality that differentiates their products.

System Studio, SPW, and the companion DSP Model Libraries deliver the highest performance simulation, combined with powerful analysis and debug capabilities for unmatched productivity for signal processing designers.

System Studio

System Studio is a high-performance, model-based algorithm design and analysis tool, combining unmatched simulation performance with high modeling efficiency, plus the industry's best integration into the chip implementation design and verification flows. Leading wireless companies rely on Synopsys' System Studio to address their system-level design needs. In fact, more than half of all mobile phones worldwide rely on algorithms designed with System Studio.

System Studio supports complex signal processing functions such as multi-antenna receiver algorithms, multimedia processing, and communication standards compliance. It offers a rich set of analysis functions that help address the imperfections introduced by transmission, non-ideal analog components, and fixed-point digital implementation in speech, multimedia and Internet connectivity.

Its unique dataflow simulation engine provides the simulation performance necessary to explore multiple design scenarios in a short period of time. Its fixed-point simulation acceleration sets it apart from any other solution on the market, achieving a speed improvement of 10X for typical mixed floating-point/fixed-point simulations and up to 200X for fixed-point only simulations.

Key benefits

- Model-based design
- Multi-rate, dynamic dataflow
- Extended finite state machines
- IEEE 1666 SystemC™ at all levels of abstraction
- Fast simulation performance
- Vector-based processing
- Analog and digital waveforms, eye and scatter diagrams, histogram, monitors and much more
- All major HDL simulators supported

SPW

Synopsys SPW (Signal Processing WorkSystem) is the fastest path from innovation to implementation for digital signal processing systems, applying a model-based design approach. At its core is the C data flow (CDF) modeling paradigm which enables the most efficient description of digital signal processing systems which may be implemented in dedicated digital hardware or embedded software. CDF is an intuitive way of describing highly-parallel systems which can produce a fully deterministic execution schedule, critical for the design of today's heterogeneous, multi-core platforms. Implementing complex digital signal processing systems for consumer, infrastructure, medical, automotive and aerospace & defense companies is the key challenge for innovation, since most of the design time is spent on investigating the effects of individual implementation decisions on the performance of the entire system. Pure language-based approaches (MATLAB® or C/C++) fail at these challenges as they do not constrain the modeling approach enough to improve implementation and simulation productivity.

Key benefits

- Faster innovation for digital signal processing-based products
- Reduction of design effort by modeling with CDF
- Drastic design cost reduction through systematic reuse
- Best ROI in the industry for DSP system simulation
- Proven hardware implementation path

System Studio DSP Model Libraries

The System Studio DSP Model Libraries consist of more than 3000 models ranging from simple to complex, supporting the analysis and design of advanced protocols and standards in the wireless and digital signal processing domain. These proven models accelerate digital signal processing algorithm design by providing ready-to-go simulation models that can be quickly modified to create alternative solutions, then analyzed in Synopsys' high-performance data flow modeling environment, System Studio.

- The System Studio DSP Base Library includes more than 2000 distinct signal processing models and a large number of combined examples that serve as demo vehicles or starting points for customer specific configurations. All models are provided in source code for maximum flexibility.
- Additional libraries such as the System Studio Reference Design Kit (RDK) Library, Error Correction Coding (ECC) Library, and Speech Library provide dedicated models to support the analysis and design of advanced protocols and standards in the wireless and digital signal processing domain. All models come with ready-to-use sample configurations.

For more information on System Studio visit www.synopsys.com/systemstudio.

High Level Synthesis

Synphony HLS

Synphony HLS is a language and model-based high level synthesis (HLS) technology that provides an efficient path from algorithm concept to silicon. Designers can construct high level algorithm models from math-languages and IP model libraries, and then use the Synphony HLS engine to synthesize optimized RTL implementations for ASICs and FPGAs, architectural exploration and rapid prototyping. Synphony HLS also generates high-performance C-models for system validation and early software development in virtual platforms.

Key benefits

- An automated flow from MATLAB to optimized RTL
- Automatic fixed-point conversion and fixed-point IP model library
- Synthesis of optimized RTL architectures for ASIC and FPGA
- Rapid prototyping methodology for early algorithm validation
- C-model generation for early software development and fast system validation
- Automatic generation of test vectors and scripts for RTL verification in VCS®
- Unified verification across multiple flows including prototyping and ASIC implementation

Automated flow from MATLAB language and high level IP to optimized RTL

Using a unique constraint-driven fixed-point propagation methodology, Synphony HLS allows designers to quickly and intuitively derive fixed-point models from a synthesizable subset of high level, floating-point MATLAB code. The Synphony HLS engine then synthesizes architecturally optimized RTL to meet area, speed and power goals. Synphony HLS allows designers to stay in their preferred algorithm modeling language, eliminating the need to re-code and re-verify models and enabling early system-level validation and verification.

High level synthesis from a single model

The Synphony HLS engine can synthesize optimized architectures for ASIC, FPGA, rapid prototyping or virtual platforms while maintaining coherent verification through all levels of the implementation flow. Given the user-specified target and architectural constraints, the Synphony HLS engine automatically optimizes at multiple levels by applying pipelining, scheduling and binding optimizations across language and model boundaries, including M-language, IP blocks and throughout the design hierarchy.

Synthesis of optimized RTL architectures for ASIC and FPGA

Synphony HLS includes a new advanced timing estimation capability that automatically utilizes Design Compiler® for accurate information needed in automatic pipelining and rapid timing closure for a given ASIC technology.

Synphony HLS includes advanced timing and device-specific optimizations for a broad range of FPGA families from Actel®, Altera®, Lattice® and Xilinx®. This includes optimized mapping to hardware multipliers, memories, shift registers and other advanced hardware resources in today's FPGA devices.

Rapid prototyping methodology for early algorithm validation

With Synphony HLS and Synopsys' technology-leading Confirma™ Rapid Prototyping solution, design teams can quickly create a pre-silicon prototype of their design and start high-performance algorithm validation and software development much earlier in the design cycle.

C-model Generation for Early Software Development and Fast System Validation

Synphony HLS complements C/C++ implementation, verification and embedded software development flows by making C-model creation a natural byproduct of the development flow. Synphony HLS generates fixed-point ANSI-C models that can be used in a variety of system simulation environments and virtual platforms including Synopsys' Innovator, System Studio, VCS and SystemC flows. Synphony HLS enables C-based verification and validation to start much earlier in the design cycle.

For more information on Synopsys' High Level Synthesis solutions, visit www.synopsys.com/hls

Mechatronic Systems

Mechatronic systems are comprised of a mixture of electrical power, multi-domain actuation (e.g. electromechanical or hydraulic), and electronic control. With the rising complexity of mechatronics in current automotive, aerospace, and industrial applications, virtual prototyping solutions are necessary for modeling, analyzing, and optimizing systems to meet design goals for performance, robustness, and reliability.

Saber

Saber® is the industry standard tool suite for simulating and analyzing mechatronic systems. Saber's powerful simulation technology and modeling capabilities provide designers with the ability to simulate, analyze, and verify interactions between multiple physical domains (electrical, magnetic, mechanical, thermal, hydraulic, etc.). With Saber's comprehensive suite of advanced analyses, designers can perform optimization, Robust Design, and FMEA on virtual prototypes of any system. Production proven with hundreds of successful designs in multiple industries, Saber continues to be the preferred solution for minimizing costs, reducing design iterations and increasing reliability of mechatronic systems.

Key benefits

- Model complete mechatronic systems using industry standard hardware description languages MAST® and VHDL-AMS
- Select devices from the industry's largest library (>30,000) of behavioral and characterized simulation models
- Easily reuse models described in other formats: Spice, Simulink, C/C++, and more
- Analyze and verify at the system, circuit, device or component level across physical domains
- Choose from over 60 performance measurements to quickly analyze and document simulation results
- Improve design reliability with advanced stress, sensitivity, statistical, and worst-case analyses
- Integrate with leading solutions for PCB design and embedded software design
- Automate simulation and results analysis tasks
- Increase analysis throughput with distributed simulations across multiple CPUs

Wire Harness Design

The wire harness forms the backbone of the entire electrical system of automotive and aerospace vehicles. The correct and reliable implementation of the wire harness represents one of the most expensive and technically challenging aspects of vehicle systems design.

Saber Harness provides proven design and verification capabilities in conjunction with the Saber Simulator to create correct-by-design wire harnesses. Designers can create schematic drawings and connectivity diagrams, export component and wire data, import geometry information from MCAD tools, simulate electrical functions, create bundles with connector positions and generate data for manufacturing – all within an easy-to-use design environment.

Key benefits

- Provides an integrated data flow for electrical system design from concept to manufacturing
- Analyze electrical systems before layout and manufacturing to avoid system failure in production
- Minimizes data entry and manual checking tasks, automates data processing steps while maintaining data integrity
- Integrates with popular 3D CAD tools (Catia, NX, Pro/Engineer)
- Supports team and concurrent engineering working methods, saving valuable design time and maintaining data integrity
- Verify hardware/software interaction with co-simulation
- Easy-to-use design editor

TCAD

TCAD Sentaurus

Technology Computer-Aided Design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor processing technologies and devices. Synopsys TCAD Sentaurus offers a comprehensive suite of industry leading process and device simulation tools, as well as a powerful GUI-driven simulation environment for managing simulation tasks and analyzing simulation results. The TCAD Sentaurus process and device simulation tools support a broad range of applications such as CMOS, power, memory, image sensors, solar cells, and analog/RF devices. In addition, Synopsys also offers Raphael™, an interconnect modeling and extraction tool which provides critical parasitic information for optimizing chip performance.

Sentaurus Process

Sentaurus Process is an advanced 1D, 2D and 3D process simulator for developing and optimizing silicon semiconductor process technologies. A comprehensive set of process models covers ion implantation, dopant diffusion, oxidation, mechanical stress, and geometric deposition and etching. Physical deposition and etching is available through an interface with Sentaurus Topography. An extensive advanced calibration parameter set derived from equipment vendor data and calibrations to state-of-the-art processes is also available. Sentaurus Process interfaces with Sentaurus Structure Editor and Sentaurus Topography to provide a flexible environment for creating 2D and 3D device structures.

Key benefits

- Fast prototyping, development, and optimization of a broad range of technologies with comprehensive physics-based process modeling capabilities
- Optimization of the wafer fabrication process flow during module development and process integration, leading to a reduction in engineering wafers and development time
- Provides insights into advanced physical phenomena through self-consistent multi-dimensional modeling capabilities

Sentaurus Device

Sentaurus Device is an advanced multi-dimensional device simulator. It simulates the electrical, thermal and optical characteristics of silicon-based and compound semiconductor devices. Sentaurus Device incorporates an extensive set of physical models and material parameters and simulates 1D, 2D, and 3D geometries over a wide range of analysis modes: DC, AC, transient and harmonic balance. Flexible multi-dimensional meshing engines allow users to generate structured or unstructured meshes effectively. Sentaurus Device offers a comprehensive set of options that allows for flexibility in configuring application-specific solutions. It interfaces directly with Synopsys' Sentaurus Process, Sentaurus Structure Editor and Sentaurus Workbench to provide a complete state-of-the-art TCAD simulation environment.

Key benefits

- Explore new device concepts for which fabrication processes are not yet defined

- Characterize electrical, thermal and optical behavior of semiconductor devices for fast prototyping, development and optimization of their performance
- Shorten development time by supplementing experimental data with deep physical insight from simulation
- Study sensitivity of device characteristics to process variation for optimizing parametric yields

Sentaurus Workbench

Sentaurus Workbench is a complete graphical environment for creating, managing, executing and analyzing TCAD simulations. Its intuitive graphical user interface allows users to efficiently navigate and automate the typical tasks associated with running TCAD simulations such as managing the information flow, including pre-processing of user input files, parameterizing projects, setting up and executing tool instances, and visualizing results with appropriate viewers. The use of mathematical and logical expressions serves to pre-process the simulation input dynamically.

Sentaurus Workbench includes a command and mask layout interface to create, edit and organize process flows. Higher levels of abstraction support user-defined libraries that can map wafer fabrication process modules or electrical test programs.

With Sentaurus Workbench, users can automatically generate design-of-experiment splits and can distribute simulation jobs across a computer network.

Key benefits

- Efficient and streamlined organization of simulation projects
- Minimal user interaction to automate and simplify large-scale simulations
- Convenient hierarchical representation of process simulations with support for libraries and hierarchical repositories of process recipes
- Comprehensive parameterization of simulations
- Easy-to-implement optimization and sensitivity analysis
- Advanced 1D, 2D and 3D visualization of TCAD structures and simulation results

Raphael

Raphael™ is the gold standard 2D and 3D resistance, capacitance and inductance extraction tool for optimizing on-chip parasitics for multi-level interconnect structures in small cells. As a reference field solver, Raphael provides the most accurate parasitic models in the industry. Trusted by major foundries worldwide, interconnect parasitics generated by Raphael are included as part of their design reference guides.

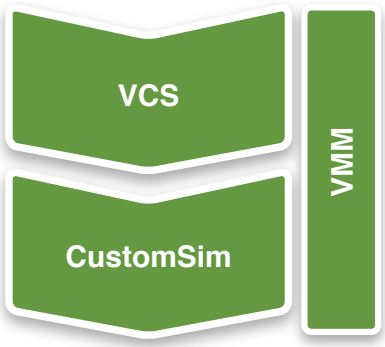
Key benefits

- Analyze complex on-chip interconnect structures and the influence of process variations
- Create a parasitic database for both foundries and designers to study the effect of design rule change
- Generate accurate capacitance rules for layout parameter extraction (LPE) tools
- Interface with Sentaurus Structure Editor to create and analyze arbitrary and complex 3D shapes using standard CAD operations or process emulation steps
- Visualize output characteristics like potential distribution inside complex 3D shapes with state-of-the-art Sentaurus Workbench Visualization tools

Verification

The Discovery™ Verification Platform is an integrated portfolio of AMS, formal equivalence checking, functional, hardware assisted, and low-power verification. Discovery provides high performance, high accuracy and efficient interactions among best-in-class technologies including mixed-HDL simulation, mixed-signal simulation, assertions, coverage, testbench automation, verification IP, formal analysis, unified debug, equivalence checking and rapid prototyping. Discovery's components support industry standards including SystemVerilog, Verilog, VHDL, SystemC™, UPF, OpenVera®, Verilog-A, Verilog-AMS, SPICE, and more.

Discovery Verification Platform



AMS Verification

Synopsys addresses the most critical issues in AMS verification. HSPICE® is employed by leading semiconductor foundries to provide designers with the gold standard for accuracy in device modeling. The CustomSim™ solution unifies Synopsys' best-in-class circuit simulation technologies to deliver superior verification performance and capacity for all classes of design, including custom digital, memory and analog/mixed-signal. For comprehensive mixed-signal verification, the CustomSim solution is tightly integrated with the VCS® functional verification solution for multi-language support, including SystemVerilog, Verilog, VHDL and Verilog-AMS.

Circuit Simulation

HSPICE

HSPICE® is the industry's "gold standard" for accurate circuit simulation and offers foundry-certified MOS device models with state-of-the-art simulation and analysis algorithms. With over 25 years of successful design tapeouts, HSPICE is the industry's most trusted and comprehensive circuit simulator. HSPICE simulates on-chip functions including: analog designs, RF design, custom digital design, standard cell design and characterization, memory design and characterization, and device model development.

As IC geometries continue to shrink, designers require a highly accurate circuit simulator to precisely predict the timing, power consumption, functionality, and yield of their designs. As board and package speeds increase, designers need to employ increasingly accurate signal integrity analysis. HSPICE includes silicon to package to board to backplane analysis and simulation to meet these critical requirements.

Key benefits

- Accuracy: HSPICE is the gold standard for accurate circuit simulation with extensive model support of the most accurate and expansive set of industry-standard and proprietary simulation models
- Performance: Synopsys has made HSPICE a performance leader. It runs post-layout simulations up to 3X faster on 1 core processor and up to 6X faster on 4 core processors with 2008.03 HSPICE. It features significant speed up for cell characterization applications, large extracted netlists, signal integrity, and 65 nm designs.
- Design for Yield: Models both device and interconnect variation and features a powerful and flexible mechanism for defining process variation effects. "Smart" Monte Carlo analysis runs several times faster than tradition Monte Carlo techniques.
- Board and package design integrity analysis: Enhanced W-elements and S-parameters model signal integrity issues and support SI Analysis. HSPICE support massive 500 port S-parameters.
- RF and High Speed Simulation: HSPICE is the best RF Simulator for PLL and VCO applications. It's also the most accurate, fastest and highest capacity RF simulator. A comprehensive solution, HSPICE simulates low noise amplifiers, power amplifiers, filters, AGC circuits, oscillators, mixers, multipliers, modulators, demodulators, and VCOs.

CustomSim

The Synopsys CustomSim™ solution delivers superior verification performance and capacity for all classes of design, including custom digital, memory and analog/mixed-signal. The comprehensive offering includes advanced analysis options for native circuit checking, power, signal and MOS reliability analysis, post-layout acceleration and mixed-signal simulation. CustomSim simplifies usability with a common set of inputs, outputs, device models and debug environment.

Designer productivity is negatively impacted by the overwhelming number of simulations that need to be run. Not only is the number of simulations increasing, but the size of circuits, combined with extracted post-layout parasitic, is far exceeding the capacity of traditional simulation solutions. Synopsys' CustomSim circuit simulation solution combines best-in-class technologies to deliver increased productivity and designer confidence to address today's AMS verification challenges.

Key benefits

- Designers can use a single solution for verifying all design types and performing advanced post-layout analysis
- Highest-performance, highest-capacity solution allows designers to run more simulations, faster
- Utilizes technology with multi-threading capabilities
- Native checking avoids wasted simulation time by flagging rule violations when they occur
- Run simulations not previously possible, for example, full-chip post-layout functional verification with CustomSim and VCS® mixed-signal simulation
- Accelerates post-layout simulation with hierarchical back-annotation
- Reuse testbenches and measurements from pre-layout simulations for post-layout verification with structural back-annotation

- Simplifies usability through a common set of inputs, outputs and device models integrated into a unified AMS verification environment

AMS Co-Simulation

The majority of today's designs contain significant analog and mixed-signal content. Even SoCs that are designed for essentially digital functions still require PLLs for timing control, digitally-controlled power management circuits, and high-speed I/O devices. To complete verification of SoCs that contain a combination of RTL and synthesized logic, along with custom digital and analog circuits, Discovery AMS analog/digital co-simulation provides a direct kernel integration between Synopsys CustomSim™, VCS® and VCS-MX.

Discovery AMS provides a comprehensive environment that enables verification of full-chip mixed-signal designs with built-in support for Verilog-AMS language defined by the Accellera 2.0 standard. It provides a unique combination of accuracy, performance and capacity with the flexibility of simulating design abstractions in any combination of Verilog, VHDL, SPICE, Verilog-A and Verilog-AMS.

Key benefits

- Built on the industry-standard PLI 2.0, providing an interface to compliant Verilog simulators, including Synopsys VCS, Cadence NC-Verilog, and Mentor ModelSim
- Co-simulation executes as a single process
- Interface A2D and D2A elements inserted automatically
- Automatic voltage level detection automatically identifies voltage levels at interface nodes
- Supports user's choice of flows

HSIM^{plus} with Circuit Check

HSIM$^{plus™}$ with Circuit Check helps users to avoid wasted simulation time by finding design and performance problems automatically, reporting potential problems in a circuit before running simulation. Circuit Check (CCK) increases verification coverage and discovers potential trouble spots that simulation misses. Circuit Check scans the netlist for common geometrical and electrical parameter errors. CCK finds hookup and bias errors before and during simulation. CCK prevents time-consuming debug problems, traces logic paths and performs static transistor-level timing analysis.

SpiceCheck

SpiceCheck is a programmable transistor-level netlist-driven static design checker. The check functionality is fully customizable based on a rich set of Tcl check commands. The program accepts flat and hierarchical netlist input and allows access to design properties including device parameters, process models, design connectivity and power domain information.

The efficient static approach in SpiceCheck helps designers quickly identify critical multi-supply design issues such as missing level-shifters and isolation gates. The programmable environment allows the check functions to be easily adapted to different design styles and disciplines. Additionally, the waveform processing capability in SpiceCheck facilitates complex design analysis using results from dynamic simulations.

It finds difficult to detect problems like missing level shifters in multi-rail designs, constant-on leakage paths, and missing or problematic ESD circuitry. Full Tcl programmability coupled with built-in verification rules makes SpiceCheck flexible for different design types yet delivers out-of-the-box productivity.

Key benefits

- Design traversal with flexible selective access
- Full access to device and net properties
- Inquiry of design connectivity
- Static DC power domain estimation
- Automatic netlist-driven topology finder
- CMOS signal path tracing
- Correlation between extracted and ideal netlist
- Total parasitic resistance calculator
- Cross-reference to dynamic waveforms
- Interactive check result browser

Spice Explorer

Spice Explorer addresses the need for an effective transistor-level debugging environment. The tool provides a netlist-driven debugging and visualization modules. Spice Explorer features SPICELint overview design browsers, the CellView Window, a graphical sub-circuit visualization with port connectivity and bias conditions, the Analysis Command Environment (ACE), and multiple utilities.

Custom WaveView

Custom WaveView is a waveform analysis tool developed for analog/mixed-signal IC designers. It provides a wide range of analysis functions and offers the best format support in the industry. The program can be used as a stand-alone application, or as an integrated part in SpiceExplorer debugging environment. The environment provides front-to-back productivity solutions to speedup verification cycle and reduces total design cost.

Custom WaveView offers the capacity and performance to process large waveform files for viewing and summarizing simulation results. With 64-bit file system support and high-performance proprietary WDF waveform compression technology, it significantly cuts down the time required to display and analyze enormous amount of simulation data from today's advanced SoC designs.

Key benefits

- Unified viewer for analog/mixed-signal simulations
- Comprehensive waveform format support
- Fastest loading speed

Formal Equivalence Checking

Synopsys offers powerful tools that address the need for equivalence checking of large, complex SoCs, all types of memories, full custom logic and I/Os. With unique and patented technologies, including Hier-IQ, datapath targeted solvers and symbolic simulation, users obtain the most comprehensive equivalence coverage available. The Synopsys formal equivalence checking suite includes Formality® for complete synthesis-flow verification and ESP-CV for full-custom, memory verification. Formality and ESP-CV offer leading performance, are easy-to-use and combine to provide full-chip, RTL-to-transistor coverage.

ESP-CV

ESP-CV verifies that two different design representations are functionally equivalent. These designs may be described as Verilog behavioral models, RTL, UDP's, gates, transistors, or SPICE netlist views.

ESP-CV is based on patented symbolic simulation technology that combines the power of formal methods with proven event-driven simulation technology. ESP-CV leverages symbolic simulation to a concept known as sequential equivalence checking to dramatically increase the quality of functional verification.

ESP-CV simultaneously simulates two different design representations using symbolic inputs while observing the outputs of each representation to assure equivalent responses. Instead of applying all possible combinations of binary states, ESP-CV applies a symbol that represents all possible input states. This results in coverage of 2N possible states with only N number of symbols.

Key benefits

- Supports any constructs from the Verilog language, including behavioral structures, such as fork, join, task, etc.
- Transistors are native to ESP-CV. It does not depend upon gate extraction or pattern matching techniques
- Supports asynchronous clocks, pulsed logic and self-timed logic
- Verifies functional equivalency of designs with different structures without any dependency on isomorphic state mapping
- ESP-CV provides fast and complete coverage, enabling users to quickly find bugs and have the confidence that the reference model is functionally identical to the transistor model
- ESP-CV increase productivity. Users no longer have to derive directed and random tests or have a long delay in releasing models while they complete their verification suites
- ESP-CV directly verifies the SPICE netlist, eliminating the need to manually extract transistor network into a gate-level representation

Formality

The size and complexity of today's designs, coupled with the challenges of meeting timing, area, power and schedule, requires that the newest, most advanced synthesis optimizations be fully verifiable. Formality® is an equivalence-checking (EC) solution that uses formal, static techniques to determine if two versions of a design are functionally equivalent. Formality supports all of the out-of-the-box DC Ultra™ optimizations and provides the highest quality of results that are fully verifiable. It supports verification of power-up and power-down states, multi-voltage, multi-supply and clock gated designs.

Formality's easy-to-use, flow-based graphical user interface and auto-setup mode helps even new users successfully complete verification in the shortest possible time.

Formality delivers superior completion on designs compiled with DC Ultra, which uses Topographical technology to achieve accurate correlation with post-layout timing, area and power, and provides advanced optimizations such as retiming, phase inversion and ungrouping. Formality is also fully compatible with DC Graphical used to predict and alleviate routing congestion. Designers no longer need to disable DC Ultra's powerful optimizations to get equivalence checking to pass. DC Ultra combined with Formality delivers maximum quality of results (QoR) that is fully verifiable.

Key benefits

- Perfect companion to DC Ultra – supports all DC Ultra default optimizations
- Intuitive flow-based graphical user interface
- Verifies low-power designs including power-up and power-down states
- Auto setup mode reduces "false failures" caused by incorrect or missing setup information

- Built-in distributed verification boosts performance
- Automated guidance boosts completion with DC Ultra
- Verifies full-custom and memory designs when including ESP technology

Functional Verification

Synopsys offers a complete functional verification solution to address increases in the size and complexity of today's RTL designs. Meeting these challenges requires advanced technologies, multicore performance, proven methodologies and fully integrated debug to ensure the highest design quality. The Synopsys suite of Functional Verification tools are tightly integrated, best-in-class technologies that allow designers to find bugs quickly and easily, significantly improving the quality of the most complex designs and enabling first-pass silicon success. These tools include the VCS® functional verification solution, Magellan™ for formal hybrid verification, the VCS Verification Library (Verification IP), Pioneer-NTB with Vera® for testbench automation, Leda® for static checking and MVSIM and MVRC for multi-voltage simulation and rule checking.

VCS

VCS®, with multicore technology, delivers delivers a 2X verification speed-up that helps users find design bugs early in the product development cycle. VCS multicore technology cuts down verification time by running the design, testbench, assertions, coverage and debug in parallel on machines with multiple cores. The combination of performance; advanced bug-finding technologies; Echo testbench coverage convergence for faster closure; a built-in debug and visualization environment; support for all popular design and verification languages including Verilog, VHDL, SystemVerilog, OpenVera, and SystemC™; and the proven VMM methodology help VCS users develop high-quality designs. The VCS solution's advanced bug-finding technologies include full-featured Native Testbench (NTB), complete assertions, and comprehensive code and functional coverage, to find more design bugs faster and easier. Additionally, the VCS Verification Library provides high-quality VIP for today's most popular bus standards. The VCS solution's powerful debug and visualization environment minimizes the turnaround time to find and fix design bugs. VCS with MVSIM and MVRC delivers innovative voltage-aware verification techniques to find bugs related to modern low-power designs.

Key benefits

- VCS multicore technology allows users to cut down verification time for long-running tests. VCS allows design-level parallelism (DLP) and application-level parallelism (ALP). DLP enables users to concurrently simulate multiple instances of a core, several partitions of a large design, or a combination of the two. ALP allows users to run testbenches, assertions, coverage and debugging concurrently on multiple cores.
- Full-featured, native testbench and SystemVerilog support
- VCS NTB provides built-in natively-compiled support for full featured SystemVerilog and OpenVera testbenches, including object-oriented, constrained-random stimulus and functional coverage capabilities
- The VCS solution's powerful testbench engines are complemented by the proven VMM methodology, defined in the popular Verification Methodology Manual for SystemVerilog, and layered testbench architecture that enables both new and experienced verification engineers to quickly create and deploy advanced, reusable, efficient verification environments
- The native assertion technology in the VCS solution enables an efficient methodology for deploying design-for-verification (DVF) techniques
- Echo testbench coverage convergence technology that reduces the time it takes to reach full stimulus functional coverage
- The VCS solution provides high-performance, built-in coverage technology to measure verification completeness
- The VCS solution includes the Discovery Visualization Environment (DVE), a next-generation, full-featured debug and visualization environment

Magellan

Magellan™ is a hybrid RTL formal verification product that allows engineers to find exhaustive proofs of design correctness and deep corner-case bugs quickly, resulting in shortened functional verification cycles and high-quality designs. Magellan's unique hybrid architecture combines the strengths of advanced formal engines with the strengths of a built-in VCS® simulation engine to verify properties on large and complex designs. Unlike pure formal tools that don't integrate with a simulator and can't reach deep design states, Magellan's automatic and transparent orchestration between VCS and its formal engines enables it to switch back and forth between simulation to get deep into the design and launch exhaustive formal searches from promising states.

Key benefits

- High-capacity formal verification using hybrid architecture
- Formal verification of user-specified properties
- Formal verification of automatically extracted structural properties
- Extensive support for assertion IP and library boosts verification productivity

- Grid-mode enables multiple proof engines to be simultaneously run on a server farm
- Same coverage database as VCS

VCS Verification Library

As the standard interfaces on SoC designs continue to increase in number and complexity, verification engineers are faced with tremendous challenges. Synopsys is leading the effort to solve these challenges with Verification IP, which simplifies testbench development, provides better coverage and delivers significant improvements in simulation runtime performance.

The VCS® Verification Library builds on the proven DesignWare® Verification IP by adding support for the Verification Methodology Manual (VMM) for SystemVerilog using the Reference Verification Methodology (RVM). Support for Native Testbench in VCS provides up to 5X improvement in runtime performance.

The VCS Verification Library is the industry's broadest portfolio of standards based verification IP which integrates easily into Verilog, SystemVerilog, VHDL and OpenVera® testbenches to generate bus traffic and check for protocol violations. Monitors provide coverage reports to show functional coverage of the bus protocols.

Key benefits

- Broadest verification IP portfolio in the industry
- Delivers 5X simulation performance improvement with VCS
- Supports proven verification methodology for SystemVerilog
- Includes example testbenches to accelerate learning and speed testbench development
- Improved ease of use for faster testbench development
- Enhanced configurability, resulting in better control and faster development of tests

Pioneer-NTB

Pioneer-NTB is a full-featured SystemVerilog testbench automation tool for use with popular VHDL and Verilog simulators. Pioneer-NTB enables engineers to easily adopt advanced verification methodologies using open standards in mixed-simulation environments. Pioneer-NTB is built on the powerful, production-proven technologies of Synopsys' VCS® comprehensive RTL verification solution and the Vera testbench automation tool, and provides instant access to the extensive VCS and Vera® ecosystems. Pioneer-NTB also supports the OpenVera language, enabling existing Vera verification environments to be easily migrated to Pioneer-NTB for up to 2X faster verification runtime performance.

Key benefits

- Support for SystemVerilog verification features enables the creation of highly effective testbench environments using object-oriented techniques, advanced data types, constrained-random stimulus, functional coverage and assertions
- Support for Synopsys' Reference Verification Methodology (RVM) and included building-block libraries accelerate the creation of robust, reusable verification environments following industry-best practices for coverage-driven, constrained-random and assertion-based verification techniques
- Built-in, complete support for SystemVerilog assertions (SVA), a library of over 50 ready-to-use checkers, and a library of assertion IP for many popular interface protocol standards, enable fast deployment of an assertion-based design-for-verification (DFV) methodology to speed bug detection and increase design quality
- Built-in functional and assertion coverage metrics and unified coverage reporting provide a comprehensive view of verification goal attainment
- Fast, native support for the VCS Verification Library of high-quality verification IP speeds development and execution of advanced verification environments for designs incorporating a wide range of standard interface protocols
- Extensive support of the OpenVera language enables Vera users to easily migrate existing verification environments to Pioneer-NTB for up to 2X faster performance

Leda

Synopsys' Leda® is a programmable design and coding guideline checker that delivers full chip mixed-language (Verilog and VHDL) and mixed representation (RTL and gate) capabilities to speed development of complex system-on-chip (SoC) designs. Leda's pre-packaged rules greatly enhance a designer's ability to check HDL code for synthesizability, simulatability, testability, reusability, and RTL/gate signoff. Leda detects clock synchronization-related bugs, isolates hard-to-time circuits, verifies layout considerations, and improves DFT for higher ATPG coverage. Leda comes prepackaged with rules to improve performance of Synopsys tools, such as VCS® MX, Design Compiler® and Formality®.

Key benefits

- Finds complex bugs, such as those associated with multiple clock domains using static analysis
- Verifies consistency of design and SDC constraints for Design Compiler®, PrimeTime® and Astro®
- Finds design and coding guideline bottlenecks that impact simulation, synthesis, timing, DFT, ERC, and layout

- Enables design reuse with prepackaged guidelines, such as the Reuse Methodology Manual (RMM), DesignWare® and StarRC™
- Implements company specific guidelines by graphically configuring prepackaged rules
- Create complex custom rules for syntax, semantic and hardware by reusing source code of the prepackaged rules
- Tcl for fast prototyping and C for up to 100X performance when implementing complex hardware rules

MVSIM with VCS

MVSIM with VCS® is a voltage-aware simulation solution that accurately verifies low-power designs and finds bugs in the architecture and implementation of power management functions. It takes in an RTL or synthesized netlist along with the power specification in IEEE 1801 Unified Power Format (UPF) as well as a low-power testbench. The powerful, built-in low-power assertions within MVSIM monitor the design for power violations and report them whenever they happen. The voltage-aware simulation results in its ability to verify the most advanced low-power designs because all voltage events are understood and accurately simulated.

Key benefits

- Accurate simulation of designs with Power Gating and many flavors of Retention
- Voltage-level aware simulation accurately verifies designs with Low-Vdd Standby and DVS
- Infrastructure to model and correctly simulate multi-rail designs leads to increased bug detection for multi-voltage designs
- Built-in, automated assertions derived from analysis of the design and power intent mitigate the risk of undetected bugs and increase verification productivity
- Automated coverage tracking and reporting helps track verification progress
- Production proven for IEEE 1801 (UPF) shows support for industry-standard power intent format

MVRC

MVRC is a multi-voltage, static low-power rule checker that allows engineers to rapidly verify the designs that use voltage control techniques for power management. MVRC also helps to pipe-clean the power intent with the IEEE 1801 Unified Power Format (UPF) before starting implementation of the low power design. MVRC's static checks ensure that implementation is consistent with the power intent throughout the design flow. MVRC can operate on an RTL, synthesized, placed and routed netlist or a transistor-level representation of the design.

MVRC's output can be viewed in a GUI that classifies messages as errors, warnings and infos and allows the user to customize the report. The GUI also facilitates cross-probing of errors, which are then highlighted in a schematic view.

Key benefits

- Power Intent Consistency Checks: Syntax and semantic checks on UPF that help validate the consistency of UPF before beginning implementation
- Architectural Checks: Global signals violating power architecture can be detected at the RTL
- Structural and Power and Ground (PG) Checks: Validate insertion and connection of isolation cells, power switches, level shifters, retention registers, and always-on cells throughout the implementation flow
- Functional Checks: Validate the correct functionality of isolation cells and power switches
- Transistor Checks: Detect sneak leakage paths, incorrectly or redundantly buffered inputs and stacking violations

Virtual Platforms

Virtual prototypes are fast simulated models of an electronic system and are used for software development, integration and test, and verification. They can be available months before first silicon is available. Their packaging and distribution enables concurrent hardware and software engineering within and across companies. Virtual Prototypes provide significant benefit because the dependency on physical hardware availability is removed. They complement traditional software development tools, with debug and analysis tools that provide unmatched visibility and controllability into the behavior of the electronic system both hardware and software. Synopsys provide a complete solution including models, tools, methodologies and services for the creation and use of virtual prototypes.

Virtual prototypes are generated from DesignWare® System-Level Library models, Innovator and System-Level Modeling services, as needed. The Synopsys DesignWare System-Level Library provides product development teams with a comprehensive set of standards-based, tool-independent transaction-level models that serve as the building blocks of virtual prototypes, see page 17 for more information. Synopsys Innovator is a SystemC-based integrated development environment (IDE) for virtual prototypes developers to efficiently integrate, analyze and verify transaction-level models (TLMs), see page 15 for more information. Synopsys has an extensive and successful track record of collaborating with customers to create and deploy transaction-level models and

virtual prototypes for their early software development, see page 44 for detailed information.

Hardware Assisted Verification

Confirma Rapid Prototyping Platform

The Confirma™ platform is a complete suite of tightly integrated, easy-to-use products for rapid prototyping including FPGA-based prototyping systems and boards, interface and memory boards, and implementation and debug software. The Confirma platform dramatically accelerates functional verification of ASIC, ASSP and SoC designs and is ideal for design and verification teams who leverage FPGA-based prototypes to improve their time-to-market and avoid costly device re-spins. The Confirma platform helps design teams to find even the hardest-to-find hardware bugs, start software development earlier in the design cycle and integrate hardware and software well ahead of chip fabrication.

The Confirma platform includes: HAPS™ High-performance ASIC Prototyping System; Certify® multi-FPGA implementation and partitioning tool; Identify® Pro debugging and visibility enhancement software; Synplify® Premier single FPGA implementation and rapid prototyping software; and CHIPit® automated rapid prototyping system.

HAPS High-performance ASIC Prototyping System

The HAPS™ High-performance ASIC Prototyping System is part of the Synopsys Confirma™ Rapid Prototyping Plus Platform. The HAPS products consist of high performance prototyping boards that are ideal for use in system validation and embedded software development.

HAPS is a modular and expandable FPGA-board system consisting of a selection of off-the-shelf motherboards and either off-the-shelf or custom designed daughter boards which can be connected in a variety of ways to accommodate and support many design styles and requirements. The motherboards vary in size from one-FPGA to multiple FPGA interconnected devices. The connections between FPGAs in the multi-FPGA motherboards can, if needed, be expanded by adding standard interconnect boards. These daughter boards connect via two or more HapsTrak™ connectors, thus adding additional wires between the FPGAs. This unique modularity of the HAPS prototyping system enables the reuse of the same motherboards for several projects or configurations, simply by adding or replacing daughter boards or subsystems.

Key benefits

- Solid and reliable with built-in self-tests check for hardware errors on power-up
- Real-time temperature and voltage monitoring prevents overheating during operation and ensures that designs run on fault-free boards and within hardware specifications
- HAPS motherboards connect to the external world via HapsTrak connectors, global clocks and local clocks, global signals, some GPIOs for testing purposes and JTAG for configuration and debug. Various types of memory and interfaces to Ethernet, USB, PCI Express, SATA, ARM®, video and logic analyzers are some of the functions available through the use of optional daughter boards
- All global clocks within the HAPS systems are individually buffered and optimized for low skew. PLLs provide flexible clocking capabilities, as well as low-skew, multi-board synchronization

CHIPit

The CHIPit® rapid prototyping systems feature a programmable interconnect architecture for more automated design implementation and enabling use modes and debug capabilities. Based on the latest FPGA technologies and complemented by an integrated set of tools, including comprehensive debug capabilities, the modular CHIPit systems can be used in diverse verification modes giving design engineers unprecedented productivity and flexibility to verify chip implementation and system functionality, thereby significantly reducing overall verification time.

Key benefits

- Innovative system architecture
- Highest flexibility with 3D Switching Technology
- Open system architecture
- Productive design implementation
- Powerful communication system
- Extensive debug capabilities
- Co-simulation with standard RTL simulators
- SCE-MI 1.1 & 2.0 compliant transaction-based verification
- In-circuit prototyping mode

Certify

The Certify® software is the leading multi-FPGA implementation and partitioning tool for ASIC designers who use FPGA-based rapid prototypes to verify their designs. Certify provides a quick and productive method for partitioning large ASIC designs onto multi-FPGA rapid prototyping boards and includes powerful features that make it easy to adapt to existing device flows, speeding the verification process and helping to ease time-to-market challenges.

Key benefits

- Includes easy to use graphical user interface (GUI) flow guide
- Fully scriptable
- Automatic gated clock conversion
- Allows automatic and/or manual partitioning
- Supports Synopsys Design Constraints for timing management
- Tightly integrated with Confirma™ hardware
- Supports multi-core parallel processing for faster runtimes
- Supports most leading FPGA devices
- Includes industry standard Synplify Premier synthesis engine

Synplify Premier

The Synplify® Premier solution is the industry's ultimate FPGA implementation and debug environment. It provides a comprehensive suite of tools and technologies for advanced FPGA designers as well as ASIC designers who use single FPGA-based prototypes. The Synplify Premier software is a technology independent solution that addresses the most challenging aspects of FPGA design including timing closure, logic verification, IP usage, ASIC compatibility, DSP implementation, debug, and tight integration with FPGA vendor back-end tools.

The Synplify Premier product offers the most efficient method of design implementation and debug. It provides in-system verification of FPGAs, dramatically accelerates the debug process, and provides a rapid and incremental method for finding elusive design problems.

Key benefits

- Fast Synthesis Mode for quick turnaround
- Integrated RTL debug with advanced triggering
- Prototyping features including DesignWare® support and gated clock conversion
- Fast timing closure through physical synthesis
- Vectorless switching activity (SAIF) generation
- Optional Design Planner for creating floor plans
- Superior QoR

Identify

The Identify® RTL Debugger is a software tool that allows users to verify and debug their FPGA design or FPGA-based rapid prototype directly from the source RTL. Identify allows users to probe any signal in the design, specify complex trigger conditions and verify the design at full hardware speed and with real-world stimulus.

The Identify tool allows users to navigate designs graphically and mark signals directly in RTL as probes or sample triggers. After synthesis, results are viewed in the RTL source code or in a waveform. Design iterations are rapidly done using incremental place and route. Identify software is closely integrated with synthesis and routing tools for a seamless development environment.

Key benefits

- Instrument and debug FPGAs directly in RTL source code
- Complex instrumentation including state machine and qualified sampling
- Internal design visibility at full speed
- Fast, Incremental debug iterations
- Technology independent—the Identify tool supports devices from Actel, Altera and Xilinx

Identify Pro

The Identify® Pro software, featuring Synopsys' TotalRecall™ technology, provides designers with full visibility into complex FPGA designs and FPGA-based ASIC prototypes enabling them to find bugs at hardware speed and analyze the cause of errors in a familiar simulation environment. Identify Pro software is complementary to other verification methodologies, such as assertion-based verification and simulation, significantly improving the overall productivity.

The Identify Pro software adds advanced triggering and full visibility to FPGA-based prototyping systems, thus making it feasible to detect hard-to-find and sporadic bugs quickly. Upon occurrence of the error condition, Identify Pro software creates the necessary simulation environment including a testbench, so that the bug can be analyzed, fixed and verified in the user's familiar RTL simulation environment. The Identify Pro tool allows users to capture the logic state and the input sequence to the design in hardware just prior to a failure and then simulate and replay the error condition using a standard RTL simulator.

Key benefits

- Full visibility into the design under test
- RTL source code debug
- Automatic test bench generation
- Assertion synthesis and assertion debug
- Technology independent–the Identify Pro debugging and visibility enhancement tool supports devices from Actel, Altera, Lattice and Xilinx

Synphony HLS

Synphony HLS is a language and model-based high level synthesis (HLS) technology that provides an efficient path from algorithm concept to silicon. Designers can construct high level algorithm models from math-languages and IP model libraries, and then use the Synphony HLS engine to synthesize optimized RTL implementations for ASICs and FPGAs, architectural exploration and rapid prototyping. In addition, Synphony HLS also generates high-performance C-models for system validation and early software development in virtual platforms.

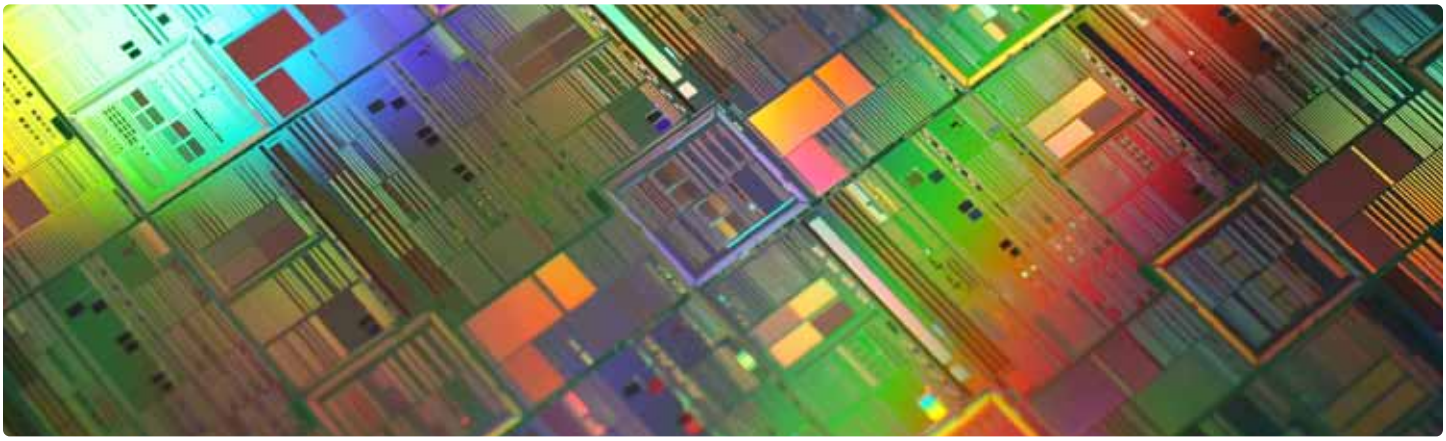
Key benefits

- An automated flow from MATLAB to optimized RTL
- Automatic fixed-point conversion and fixed-point IP model library
- Synthesis of optimized RTL architectures for ASIC and FPGA
- Rapid prototyping methodology for early algorithm validation
- C-model generation for early software development and fast system validation
- Automatic generation of test vectors and scripts for RTL verification in VCS®
- Unified verification across multiple flows including prototyping and ASIC implementation

Low Power Verification

Power-aware verification (analog and digital) is the leading concern for designs at 65 nm and below. For voltage-aware functional verification, the Eclypse™ Low Power Solution includes VCS® with MVSIM, a voltage-aware simulation engine, as well as MVRC, a voltage-aware static checker that offer comprehensive coverage for all power management functions. The voltage-aware nature of MVSIM and MVRC provide the needed accuracy and verification coverage for power-managed designs. Effects such as power state transition analysis, power shutdown, power rules checking, etc. are performed. HSPICE® and CustomSim™ test for non-digital effects, such as leakage power, floating nodes, and dynamic IR drop. The overall result is a completely verified power-managed design.

IP



DesignWare Intellectual Property

Synopsys is a leading provider of high-quality, silicon-proven interface and analog solutions for SoC designs. Synopsys' broad IP portfolio consists of:

- Complete connectivity IP solutions consisting of controllers, PHY and verification IP for the industry's most widely used protocols such as USB, PCI Express, DDR, SATA, HDMI, MIPI and Ethernet
- Analog IP including Analog-to-Digital Converters (ADCs), Digital-to-Analog Converters (DACs), Audio Codecs, Video Analog Front Ends and Touch Screen Controllers
- The DesignWare® Library containing over 150 essential infrastructure IP for design and verification
- The DesignWare minPower Components which offer unique, power-optimized datapath architectures that reduce dynamic and leakage power for mobile devices and high-performance applications
- SystemC™ transaction-level models that enable the development of virtual platforms for rapid, pre-silicon development of software

With a robust IP development methodology, extensive investment in quality and comprehensive technical support, Synopsys enables designers to accelerate time-to-market and reduce integration risk.

Interface IP

Synopsys provides designers with complete, silicon-proven IP solutions consisting of digital controllers, PHY and verification IP for standard interfaces such as USB, PCI Express, DDR, HDMI, SATA, MIPI and Ethernet. As a leading provider of connectivity IP for over a decade, Synopsys offers a comprehensive portfolio of interface IP solutions that are optimized for low power and small area, and have gone through extensive interoperability and compliance testing. With millions of units shipping in volume, designers can trust that the IP can be integrated into their SoCs with significantly less risk.

USB

The DesignWare® USB IP portfolio consists of digital controllers, PHY and verification solutions for the USB 1.1, 2.0 and 3.0 specifications. Synopsys DesignWare USB IP helps designers reduce the risk and the cost of integration by providing high-quality, silicon-proven solutions optimized for low power and small area to meet the demands of today's mobile and consumer electronic applications. Certified over 300 times, by both Synopsys and its customers, the DesignWare USB IP solution is the most certified solution in the industry, has been implemented in over 2000 designs and in more than 50 different process technologies ranging from 130 nm to 28 nm.

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PCI Express

Synopsys DesignWare® IP solution for PCI Express consists of a suite of digital controllers for all port types including Endpoint, Dual Mode, Root Port & Switch Bridge, PHY IP supporting process technologies from 130 nm to 40 nm, and VIP. All of the IP are compliant to the PCI Express 3.0, 2.0, 1.1 and PIPE specifications. These products enable designers to lower integration risk by offering a PCI Express solution that has been implemented in over 300 SoC designs, has gone through extensive third-party interoperability testing and is shipping in volume production. The DesignWare IP for PCI Express targets desktop, mobile, consumer and communication SoCs.

DDR

The DesignWare® DDRn Memory Interface is a family of system-level IP solutions for SoCs requiring an interface to the broad range of high-performance DDR3, DDR2, DDR, Mobile DDR, and LPDDR2 SDRAM memory subsystems. These solutions are designed to minimize integration efforts while offering flexible solutions that are tailored to the end application. Optimized for improved data bandwidth, low power and enhanced signaling features, the DesignWare DDRn IP solutions include a choice of scalable digital memory and protocol controllers, and an integrated hard macro PHY delivering memory system performance of up to 2133 Mbps.

HDMI

The DesignWare® HDMI TX and RX IP solution consists of a suite of configurable digital controllers and high-speed, mixed-signal PHY IP. The HDMI IP is fully compliant to the 1.3 and 1.4 standard specifications and has gone through extensive in-house and third-party interoperability testing, enabling designers to lower integration risk. The high-performance DesignWare IP for HDMI is extremely low in power, area and is available in leading 90, 65, 45 and 40 nm process technologies with products shipping in volume.

MIPI

Synopsys' DesignWare® MIPI IP portfolio supporting popular MIPI interfaces such as DigRF, CSI-2, D-PHY and M-PHY. The DesignWare MIPI IP solutions are optimized for small area, low power consumption and are compliant to the industry standard specifications. Synopsys' DesignWare IP solutions for MIPI help designers accelerate the development of next-generation mobile devices that require high-bandwidth connectivity and support for multi-megapixel cameras.

SATA

The complete, silicon-proven DesignWare® SATA IP solution consists of configurable host and device digital controllers, PHYs in leading processes from 130 nm to 40 nm and verification IP. The comprehensive SATA IP solution supports the 1.5, 3.0 and 6.0 Gb/sec transfer speeds and has passed the SATA International Organization (SATA-IO) Building Block interoperability testing, an independent demonstration of full SATA functionality. Synopsys' DesignWare SATA IP solution is compliant to the SATA 2.5/2.6 and AHCI specifications (including eSATA).

Ethernet

The silicon-proven DesignWare® Ethernet IP solutions consisting of the 10/100 MAC, 10/100/1G MAC, 1G/2.5G/10G MAC, Ethernet PCS digital controllers and verification IP are compliant with the IEEE specifications and shipping in volume production. The flagship DesignWare Ethernet 10/100/1G IP solution offers support for the IEEE 1588 specification, Energy Efficient Ethernet specification and ARM AMBA 3 AXI interface. In addition, a QoS module can be added to the 10/100/1G MAC, which incorporates the new audio video bridge feature. The DesignWare Ethernet 10/100/1G IP solution has been certified by the University of New Hampshire Interoperability Lab (UNH-IOL), demonstrating proven interoperability and conformance to the IEEE standards.

AMBA

The Synopsys DesignWare® IP solutions for AMBA® Interconnect protocol-based designs include a comprehensive set of synthesizable and verification IP, as well as an automated facility for subsystem assembly with the Synopsys coreAssembler tool. The DesignWare IP is fully compatible with the ARM® AMBA 2.0 and AMBA 3 AXI™ protocols, allowing flexible system architectures to fully support designers' requirements. The configurable architecture of the IP, coupled with the automated assembly tool, reduces the complexity of designing next-generation AMBA-based subsystems and significantly improves overall productivity for faster time to results.

The DesignWare Interconnect Fabric for AMBA 3 AXI includes a unique Hybrid architecture that enables the combination of dedicated high-performance channels with lower-performance shared channels. By eliminating redundant logic and wires, designers are able to realize lower area, power and reduced routing congestion.

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Mobile Storage

The silicon-proven DesignWare® Mobile Storage Host Controller IP supports the SD 2.00, SDIO 1.1, SDIO 2.0, SD 3.0, MMC 4.3, MMC 4.4, eSD and CE-ATA specifications, addressing the growing storage need for handheld and consumer electronics applications requiring low power consumption such as MP3 players, smart phones and PDAs. The comprehensive IP solution is optimized for low-power, high-performance storage devices.

JPEG

Synopsys' DesignWare® JPEG CODEC is a multimedia IP solution that enables fast and simple image compression and decompression. The CODEC encodes and decodes still or motion image data of up to four color components, according to the JPEG baseline algorithm (as specified in the ISO/IEC 10918-1 standard). The DesignWare JPEG CODEC allows for easy SoC integration into multimedia and color printing applications.

XAUI

The silicon-proven DesignWare® XAUI PHY IP is designed for use in any networking or high-end computing SoC solution. Designed for the latest high-speed backplanes, the XAUI PHY supports the 10 Gigabit Ethernet standards that are commonly used in high-speed communications applications. Based on Synopsys' proven high-speed SerDes technology, the DesignWare XAUI PHY provides a cost effective and extremely low-power solution that is designed to meet the needs of today's XAUI designs.

Analog IP

Overview

With more than 12 years of experience in delivering silicon-proven analog IP solutions, Synopsys offers designers the industry's broadest portfolio of more than 200 analog IP products consisting of analog-to-digital converters, digital-to-analog converters, touch screen controllers, audio codecs, and video analog front-ends. The DesignWare Analog IP solutions offer very low power dissipation, compact area and support for a wide range process technologies ranging from 180 nm to 40 nm, enabling the analog IP to be easily integrated into SoC designs.

Audio

Synopsys offers a comprehensive portfolio of more than 40 silicon-proven audio codec IP products for ultra compact audio (+80 dB), Hi-Fi audio (+90 dB), enhanced Hi-Fi audio (+103 dB) and advanced audio drivers. Synopsys' high-quality audio IP solutions have been implemented in over 100 customer products, are shipping in volume and are available in leading processes from 180 nm to 65 nm.

Synopsys' high-quality DesignWare® Audio IP solutions enable designers to quickly incorporate advanced audio functions into their feature-rich SoCs with reduced integration risk, while achieving the necessary performance, power and area requirements. Synopsys' robust audio IP solutions deliver performance levels similar to discrete components and significantly ease the integration effort of audio IP into embedded SoC designs.

Data Converters

Synopsys offers a comprehensive portfolio of over 100 silicon-proven DesignWare® Data Conversion IP solutions comprised of Oversampling Sigma-Delta, Pipeline, and, SAR analog-to-digital converters (ADCs), Current Steering digital-to-analog converters (DACs) and General Purpose ADCs and DACs.

The DesignWare Data Converter IP solutions are targeted at a broad range of applications such as broadband wireless and wired communications, cellular communications and video designs requiring high-performance, ultra-low power consumption and very compact area. The DesignWare Data Converter IP are available in leading foundries and advanced technology processes from 180 nm to 40 nm.

Touch Screen Controllers

The DesignWare® 10-bit, 125 kHz and the 12-bit, 1 MHz Touch Screen Controllers are flexible, very compact and power efficient controllers, built around 10-bit and 12-bit Successive-Approximation ADCs. Both controllers include the driver switches to control several types of touch screens. Both single-ended and differential (ratiometric) position measurements are supported. The DesignWare Touch Screen Controllers also feature pen touching screen detection capabilities and screen pressure measurements.

Video Analog Front-End

Today's rapidly growing home entertainment consumer market is driven by superior video quality. Analog Video Front Ends (AFEs) play a pivotal role by providing a low-power, high resolution analog interface between video devices.

Synopsys offers a comprehensive portfolio of silicon-proven DesignWare® Video AFE IP solutions that deliver high-quality video resolution (1080p/WUXGA) with minimal power consumption and small silicon area. The IP is designed to meet a wide range of analog video applications such as Standard-Definition TV (SDTV), high-definition TV (HDTV) and PC-Graphics. By providing designers with a broad portfolio of high-quality video IP, Synopsys enables designers to quickly integrate the IP into their SoCs with significantly lower risk and improved time-to-market.

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DesignWare Library

The DesignWare® Library contains the essential infrastructure IP for design and verification. With over 25,000 designers using the DesignWare Library, users can be assured that all the IP is developed with high quality and ease of use. A single license gives designers access to all the synthesizable and verification IP in the library:

- More than 100 datapath components that significantly improves design QoR
- AMBA® 2.0 AHB and AMBA 3 AXI™ On-Chip Bus fabric and peripherals
- 8051 and 6811 8-bit microcontrollers
- Verification IP for standard bus and I/Os such as PCI Express, USB and SATA
- Foundry libraries consisting of silicon-proven standard cells, I/Os and memories from TSMC Semiconductor and Chartered Semiconductor
- High-performance Star IP processor and DSP cores from providers such as IBM, NXP and Altera

minPower Components

The innovative DesignWare® minPower Components enable the reduction of specific power elements such as glitch power in deep logic levels and dynamic power in high-performance datapath pipelines. The DesignWare minPower Components offer unique, power-optimized datapath architectures that enable DC Ultra™ to automatically generate circuits that suppress switching activity and glitches, reducing both dynamic and leakage power for mobile devices and high-performance applications. Based on the actual switching activities, transition probabilities, available standard cells and analysis of possible configurations, the DesignWare minPower Components architectures are automatically configured by DC Ultra to implement the optimal structure with the lowest power consumption.

Verification IP

Synopsys' DesignWare® Verification IP helps design engineers speed testbench development time by offering a broad portfolio of the industry's most popular bus protocols such as PCI Express, USB, SATA, Ethernet, AMBA® On-Chip Bus, OCP and more. The Verification IP integrates easily into SystemVerilog, Verilog, VHDL and OpenVera® testbenches and supports advanced verification methodologies such as the Verification Methodology Manual (VMM) for SystemVerilog. The DesignWare Verification IP is available in the DesignWare Library, VCS® Verification Library or as single licenses.

IP Reuse Tools

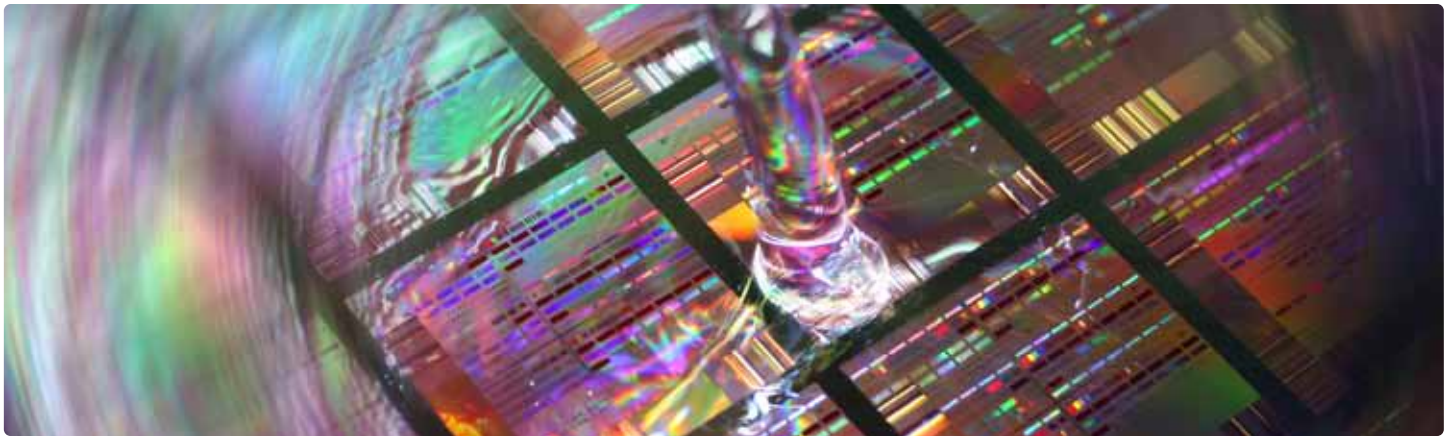
Synopsys' DesignWare® coreTools family, consisting of coreConsultant, coreAssembler and coreBuilder, enables designers to easily package, connect and configure multiple IP blocks to an on-chip bus. Using an IP-based design and verification flow with IP packaged for assembly, enables designers to minimize configuration and subsystem integration errors and significantly reduce design time.

- The coreConsultant utility walks the user through the configuration, implementation and validation of individual IP blocks packaged with coreBuilder. coreConsultant will also generate the IP-XACT file for the IP block.
- coreAssembler is an IP assembly tool that automatically generates the interconnect and configured RTL, documents the design testbench and the block and system configuration details and automatically generates an IP-XACT design file
- The coreBuilder tool, with full support for the IP-XACT specification, enables IP creators to package their IP in a format that guides the IP integrator through the configuration, implementation and verification of the IP. IP integrators can then create and begin verification of complex IP blocks and subsystems in hours, not days—greatly reducing the overall cycle time.

System-Level Library

Synopsys' DesignWare® System-Level Library provides product development teams a comprehensive set of standards-based, tool-independent transaction-level models (TLMs) that serve as the building blocks of virtual platforms. The OSCI TLM-2.0-compliant models in the System-Level Library are written in SystemC™ to function with any IEEE 1666-compliant SystemC simulator. Mirroring the productivity gains realized by IP reuse in the implementation phase, the System-Level Library accelerates the development of virtual platforms, see page 27 for more information, by providing pre-defined abstract models of hardware components in wireless, multimedia, networking and automotive application domains.

Solutions



Eclypse Low Power Solution

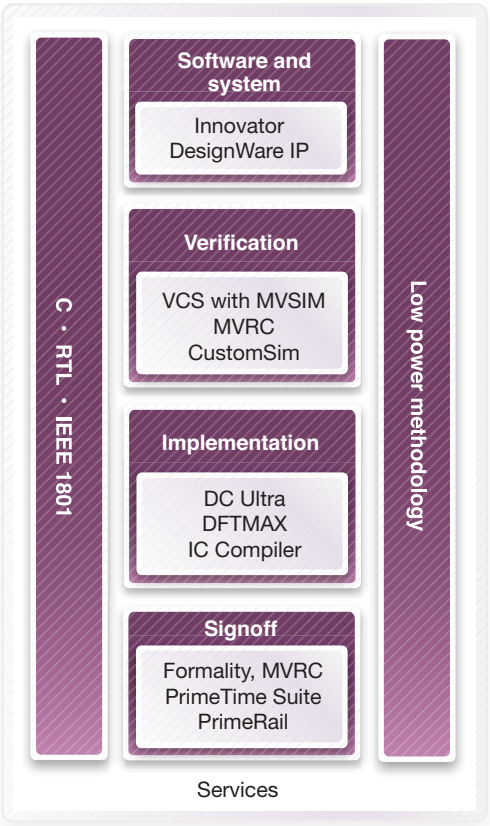
Building on more than 10 years of design leadership, the Synopsys Eclypse™ Low Power Solution incorporates leading-edge, silicon-proven, advanced low power technologies in an easy-to-use, highly automated environment. The perfect alignment of technology, methodology, intellectual property (IP), services, and industry standards, the Eclypse Low Power Solution encompasses every phase of the design process, from architectural analysis through design verification, implementation, and signoff.

The Eclypse Low Power Solution supports the IEEE 1801 Unified Power Format (UPF) standard, which is used to specify power intent requirements. It also features several new, advanced low power technologies, including:

- DesignWare® minPower Components, which provide reduced power for designs with significant datapath content with architectures and optimizations specifically targeted for low power
- Enhanced automation for power switch insertion and optimization, which allows early and accurate power planning exploration and "what-if" analysis using IR drop and area constraints
- In-Design Rail Analysis, which enhances ease-of-use by providing for the verification of power network design using signoff technology within the design planning environment

By simplifying the deployment of the latest low power techniques, such as MTCMOS and DVFS, the Eclypse Low Power Solution enables design teams to adopt advanced low power techniques while dramatically reducing time-to-results (TTR), reducing risk, and ultimately delivering the highest quality silicon in the challenge to meet the most demanding power, area, speed, and yield objectives.

Eclypse Low Power Solution



For more information, see http://www.synopsys.com/eclypse

System-to-Silicon Verification Solution

Verification is an unbounded problem, putting chip and system verification teams under tremendous pressure given constrained development budgets and schedules. The result is that while software and verification account for the vast majority of SoC budgets, inadequate analog and functional verification still account for most re-spins, and software accounts for the vast majority of product introduction delays. Waiting for first silicon to begin software development, significantly expanding verification teams or pushing back tapeout schedules are rarely viable options. Productive verification today requires a more intelligent, unified approach that integrates and leverages all phases of verification from software to silicon.

The Synopsys System-to-Silicon Verification Solution delivers powerful, proven verification technologies in an easy-to-use, highly automated environment. A comprehensive portfolio of tools, IP, methodologies, services and standards, the System-to-Silicon Verification Solution spans the entire SoC verification flow including: architecture analysis and early software development; high-performance analog, digital and mixed-signal simulation; detailed static and formal analysis; and hardware-assisted system validation. This flow is supported by productive, proven methodologies and the industry's largest portfolio of system-level and verification IP. By simplifying the deployment of advanced verification technologies, the System-to-Silicon Verification Solution enables faster, more predictable verification closure.

The System-to-Silicon Verification Solution brings together key Synopsys technologies and platforms to address all phases of SoC verification. The Solution includes Innovator virtual platforms for architecture analysis and pre-RTL software development, the Discovery™ Verification Platform for high performance functional and analog/mixed signal (AMS) verification, the Confirma™ Rapid Prototyping Platform for pre-silicon software development and system validation and the DesignWare® System-level Library and VCS® Verification Library for rapid platform and environment development. With tight links between best-in-class tools, unified IP and proven methodologies, the Synopsys System-to-Silicon Verification Solution helps SoC development teams increase productivity and meet growing verification challenges.

Virtual Prototypes

Virtual prototypes are fast simulation models of an electronic system and are used for software development, integration and test, and verification. Because they are not dependent on the availability of physical hardware, virtual prototypes can be developed months prior to first silicon, enabling concurrent hardware and software development. These virtual prototypes can also be easily distributed within and across companies to validate the hardware and software behavior of electronic systems using debug and analysis tools that are complementary with traditional software development tools. Synopsys provides a complete solution including models, tools, methodologies and services for the creation and use of virtual prototypes.

Virtual prototypes are generated from DesignWare® System-Level Library models, Innovator and System-Level Modeling services, as needed. The DesignWare System-Level Library provides product development teams with a comprehensive set of standards-based, tool-independent transaction-level models (TLMs) that serve as the building blocks of virtual prototypes, see page 17 for more information. Synopsys Innovator is a SystemC™-based integrated development environment (IDE) for virtual prototype developers to efficiently integrate, analyze and verify TLMs, see page 15 for more information. Synopsys has an extensive and successful track record of collaborating with customers to create and deploy TLMs and virtual prototypes for their early software development, see page 44 for detailed information.

For more information on virtual prototypes, see http://www.synopsys.com/virtualprototypes

Confirma Platform

The Confirma™ platform is a complete suite of tightly integrated, easy to use products for rapid prototyping including FPGA-based prototyping systems and boards, interface and memory boards, and implementation and debug software. The Confirma platform dramatically accelerates functional verification of ASIC, ASSP and SoC designs and is ideal for design and verification teams who leverage FPGA-based prototypes to improve their time to market and avoid costly device re-spins. The Confirma platform helps design teams to find even the hardest-to-find hardware bugs, start software development earlier in the design cycle and integrate hardware and software well ahead of chip fabrication.

The Confirma platform provides all the benefits of traditional hardware-assisted verification methods, but is more cost effective and efficient. The Confirma platform is ideal for ASIC/ASSP design and verification teams who want to start software development earlier in the design cycle and integrate hardware and software well ahead of chip fabrication, in order to accelerate overall time-to-market schedules.

The Confirma Rapid Prototyping platform is enhancing and augmenting traditional verification tools and methodologies by providing a highest performance environment for early, pre-silicon software development and system integration.

For more information on Synopsys' Rapid Prototyping solutions, visit www.synopsys.com/confirma.

Discovery Verification Platform

The Discovery™ Verification Platform is an integrated AMS and functional verification solution with best-in-class technologies delivering high performance and scalability, including mixed-HDL and AMS simulation, debug, native design checks, assertions, low-power verification, verification intellectual property (IP), code and functional coverage, testbench automation and formal analysis. Combined with support for industry-standard hardware design and verification languages, including SystemVerilog, Verilog, Verilog-AMS, VHDL, SystemC™, OpenVera® language, IEEE 1801 (UPF), the VMM methodology and related VMM applications, the Discovery Platform enables verification engineers to achieve significantly higher productivity and faster verification closure times for their advanced AMS and digital designs. This contributes to first-time silicon success within required project cycles. Discovery is part of the Synopsys System-to-Silicon Verification Solution, the industry's most comprehensive suite of proven embedded software development, system validation, functional verification and circuit simulation software, hardware, IP, methodologies and services for complex SoC design.

Galaxy Implementation Platform

The Galaxy™ Implementation Platform is a highly integrated comprehensive solution for cell-based and custom IC implementation. It accepts design intent in industry standard formats and generates a production ready IC design in GDSII format. Galaxy incorporates industry-leading Design Compiler® Ultra RTL synthesis, IC Compiler place and route technology, StarRC™ extraction and PrimeTime® signoff tools to concurrently balance design constraints and achieve optimal IC performance, area power and manufacturability. Augmenting these core capabilities are fully integrated design-for-test, In-Design Physical Verification and power network analysis capabilities. Galaxy is multicore-enabled to deliver faster results on the latest multicore-based compute servers.

The Galaxy Platform lets designers do what they do best—design!

FPGA Implementation

Synopsys' Synplicity family of FPGA Synthesis products have proven over many years to deliver a high-quality, fast-turnaround, technology-independent FPGA implementaion solution. This solution provides FPGA designers with the fastest time-to-results for complex FPGAs, multi-vendor support, area optimization for cost reduction, powerful design analysis, RTL debug, simulation integration, and 3rd party IP support. Synopsys FPGA implementation solution provides an array of tools and flows to take advantage of the flexibility and cost savings that programmable logic makes possible. These include:

ASIC verification using FPGA-based prototypes

As a part of Synopsys' Confirma™ Verification Platform, the Synplify® Premier solution offers the most comprehensive system for implementing FPGA-based prototypes of ASICs and ASSPs including gated clock conversion and DesignWare® support.

Integration with algorithmic synthesis for DSP

Tight integration with Synopsys' high level synthesis product (Synphony HLS) allows FPGA designers to rapidly explore and implement DSP algorithms in a range of FPGA architectures and vendors from a single model.

Fastest time-to-results for complex FPGAs

Unique timing-driven and graph-based physical synthesis technologies enable users to reach aggressive timing goals in the shortest amount of time.

Multi-vendor support

Synopsys' technology independent FPGA implementation solutions allow users to quickly retarget their designs to the FPGA architecture that makes the most sense for the project, at any time in the design cycle.

Area optimization for cost reduction

The Synplify synthesis tools let designers specify the performance they need, then the algorithms work to minimize the logic required to achieve that performance, allowing the design to fit in the smallest, least expensive part possible.

Powerful design analysis

Synopsys' FPGA solution allows designers to thoroughly analyze their RTL code by instantly creating a high level graphical representation of the design that links directly to the source code that produced it.

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RTL debug

Synopsys offers the first software tool that allows designers to instrument and debug a live, operating FPGA directly in their familiar source RTL code, rather than synthesized gates.

Third party IP

Use of IP is increasingly important to FPGA designers. The Synplify family of products supports the IP-XACT standard and has integrated access to 3rd party IP for evaluation.

Lynx Design System

The Lynx Design System is a production-ready chip implementation platform that is architected for rapid, "out-of-the-box" deployment to one or multiple project sites. It combines an open, tapeout-proven RTL-to-GDSII design flow, GUI-based runtime automation, design metrics capture and reporting, and a subsystem that automates the configuration of pre-validated foundry data.

The Lynx solution takes full advantage of the Synopsys Galaxy™ Implementation Platform, but is flexible to readily accommodate internal or third-party tools. Since Lynx encapsulates the collective experience of Synopsys and its foundry and third-party IP partners through pre-established flows, recommended tool settings and pre-validated technology data, it can be rapidly set up and operational for design teams.

The hierarchical production flow embedded in the Lynx Design System is built on a leading-edge design flow that is tapeout-proven on over a 100 designs in a wide range of applications and manufacturing processes. It is in use from older nodes to 32 and 28 nm manufacturing processes.

Lynx automates flow configuration and execution to improve the productivity of the design team. Embedded in Lynx are the best design practices from the ARM-Synopsys implementation Reference Methodologies (iRM) using ARM® physical IP optimized for ARM processors. The iRM streamlines the procedures used by designers to target ARM processors to their chosen technology nodes by delivering a comprehensive solution proven by ARM and Synopsys to enable outstanding performance and energy efficiency.

The Lynx Design System includes an intuitive and easy-to-use graphical user interface (GUI) which enables rapid configuration of the encapsulated methodologies into a customized flow. It also includes the ability to graphically execute and monitor the flow as a design progresses through it.

Using Lynx's Runtime Manager, creating a new flow or modifying existing flows is accomplished using point and click operations. Flat or hierarchical flows for a single block or for an entire chip are defined by connecting various tasks together based on their dependencies. Parallel task execution and design exploration involving multiple invocations of the same task or flows with different parameters are also easily specified.

Once defined, these flows can then be executed and their status monitored from within the GUI. Through the Runtime Manager, designs tasks can be distributed across a compute farm using industry-standard job distribution tools.

The browser-based Management Cockpit provides designers and managers platform-independent, 'on-demand' access to quality-of-results (QoR) and resource-related project metrics. Over 60 metrics are automatically acquired in a database by the Lynx Design System during flow execution, and additional user-defined metrics can be defined.

The Management Cockpit's reporting GUI provides access to all captured project metrics and specified design targets. Through an intuitive user interface, managers and designers can easily create custom reports such as: dashboards that show key project metrics such as frequency, area and power; trend analyses of design progress and comparison to target goals; current design status summary; block level comparisons of QoR data; and a summary of tools and tool versions used in the flow.

Mismatched, incorrect, or incomplete technology and library files can negatively impact project schedule and designer productivity. The risk is especially high at newer process nodes, where technology data is constantly changing. The Lynx Design System helps address these early design impediments by encapsulating the collective experience of Synopsys and its foundry and third-party IP partners in recommended tool settings and pre-validated technology data. Lynx's Foundry-Ready System includes the scripts and documentation necessary to configure and pre-test any library and technology files for proper execution in the design flow.

The Foundry-Ready System also facilitates first-time-right, manufacturing-ready tape-outs. It integrates process-specific methodologies such as metal fill and via optimization, and representative settings like on-chip variation (OCV), into the design flow. Through a combination of automated report gathering, documented guidelines, and post-GDSII reports, the Foundry-Ready System helps improve the quality of the foundry handoff and reduce the cycle time from GDSII to first silicon.

Industry Solutions

Competitive pressures highlight the value of a cohesive engineering solution. A high-value solution is tailored to address specific industry problems which results from a focus on relevant issues and the development of integrated tools and methodologies. Synopsys provides a range of solutions to address the challenges in automotive, memory, military/aerospace applications, and mobile devices.

Automotive

Electronics continue to infiltrate all aspects of automotive design as consumer demand for safety, performance, fuel efficiency, and reliability continues to grow. Automotive design relies on an efficient exchange of design information across the supply chain. Electronic design incorporates semiconductor, FPGA, PCB, sub-system, system, and software design. Integrating all these aspects of electronics requires careful attention to component design and system interactions to reduce costs and warranty recalls, meet performance specification, and enhance vehicle reliability.

Whether designers are implementing mixed-signal custom ICs, advanced FPGAs, developing sub-systems, or are responsible for systems integration for vehicle design and hardware/software co-design, Synopsys provides comprehensive design tools for today's complex automotive design chains.

Memory

Memories are one of the fastest growing segments in the electronics industry, but come under enormous cost, consumer, and competitive pressures with unpredictable fluctuations in supply and demand. These pressures and market fluctuations require memory providers to be flexible and always conscious of ways to reduce costs.

Memory designs are severely cost- and area-driven. The more bit cells that can be placed on the smallest possible area, the higher the yield. However, smaller areas and line widths cause significant problems with electrical integrity and manufacturing – problems that should be addressed early in the design cycle.

Synopsys understands the need to create highly-concentrated, low-cost memory devices that provide flexible function for today's demanding market needs. Synopsys is a technology leader in integrated circuit and SoC design and has the right tools and methodologies to deal with designers' cutting-edge design needs for IC design, verification and manufacture. Synopsys can help designers increase capacity, decrease design time, and lower production costs.

Military and aerospace

Electronics design for military and aerospace applications requires high-performance ASIC/FPGA implementation, multi-domain verification capabilities and maximum flow traceability for compliance to standards such as DO-254.

The Synopsys Mil/Aero Solution enables powerful ASIC and FPGA implementation, addresses complex verification requirements across physical domains, and facilitates the documentation and tracking needed for hardware standards compliance and certification.

Several key factors must be addressed when defining and implementing the design of IC, components, and systems that are destined for use in aerospace and/or military applications. Among these are:

- High reliability and performance to spec in extreme environmental conditions
- Implementation in ASIC or FPGA devices
- Fast, accurate and flexible prototyping
- Compliance to standards for flow documentation and repeatability
- Managing hardware/software co-design
- Verification at the functional, code and hardware levels

Synopsys offers a powerful lineup of methodologies and technologies that can aid in managing these factors successfully, and bring significant benefit to the designers of military and aerospace hardware.

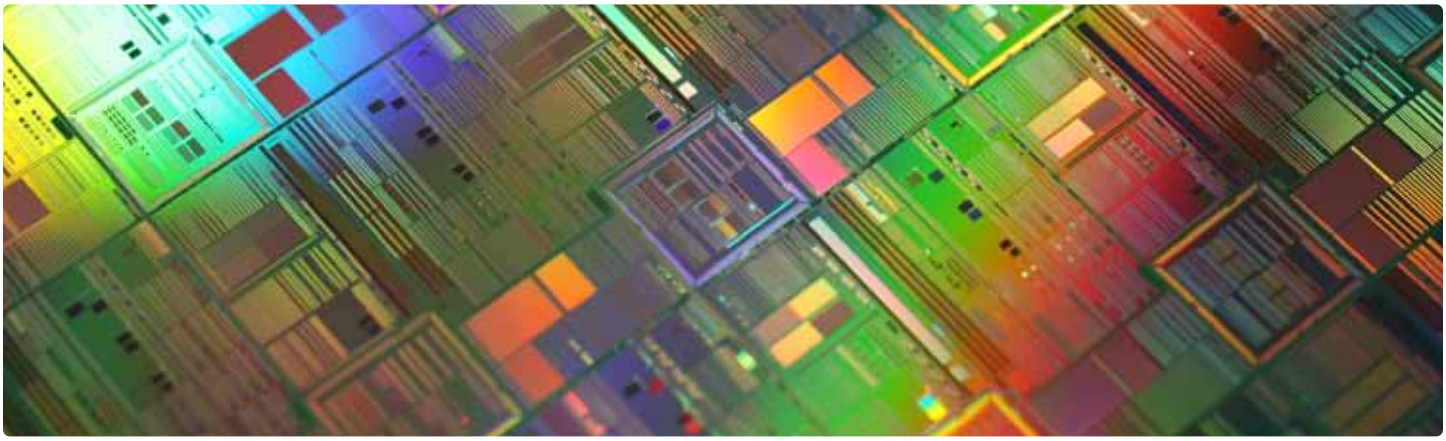
Mobile devices

Designers face numerous challenges in developing the systems and ICs needed for today's leading-edge mobile devices while adhering to tight schedules. These challenges include defining and testing new system algorithms, writing and debugging complex software in advance of finished hardware, designing SoCs to provide maximum functionality with a battery constrained power budget, and assuring that the devices can be produced at high levels of yield, quickly.

The Synopsys Mobile Devices Solution enables concurrent hardware/software co-design, addresses complex verification requirements, fosters low power design, and maximizes the manufacturability of systems and ICs for mobile devices.

Synopsys offers a powerful lineup of methodologies and technologies that have provided significant benefits for systems and IC designers at the top providers of wireless ICs and systems.

Services



Accelerating Tool and Methodology Adoption

Synopsys Professional Services is expert in Synopsys' technology-leading tools and platforms. Benefiting from our close ties to the tool developers, extensive and ongoing employee training, and a broad resume of customer project experience, our design consultants are uniquely qualified to help you rapidly deploy the latest EDA technology into your flow.

You've made the right choice. Synopsys' portfolio is the industry's leading suite of implementation and verification tools for developing complex chips. Of course, maintaining our technology leadership means that we continuously enhance our products with the most advanced features to improve designer productivity and address the latest design challenges. Synopsys Professional Services helps you take immediate and full advantage of all of Synopsys tools' capabilities and run time improvements, rapidly integrating them into your production flow and applying them in real-time to your most critical designs.

Synopsys' Accelerating Tool & Methodology Adoption services include assistance with:

- Migrating and customizing design scripts for new tool versions
- Methodology consulting to deploy design methods and best practices
- Applying new tool features through project-based design assistance:
  - Design Compiler Ultra: Library-aware mapping and structuring, data path optimization, critical path re-synthesis and topographical technology for accurate correlation to post-layout timing, area and power
  - Design Compiler® Graphical: virtual global routing technology to predict wire routing congestion during RTL synthesis
  - IC Compiler: Concurrent multi-mode, multi-corner optimization, advanced clock tree synthesis and post-route optimization, physically-aware scan-chain optimization, signal integrity (SI) and Multi-Vth leakage power optimization, multi-voltage power optimization, MTCMOS leakage optimization, yield optimization

- IC Compiler Zroute Technology: Advanced routing algorithms, concurrent DFM optimizations and multithreading
- IC Validator: In-Design physical verification
- PrimeTime Suite: A single Timing, SI and power analysis environment
- PrimeTime® SI: ILM/ETM-based hierarchical static timing analysis, delay calculation, on-chip variation (OCV), SI signoff
- PrimeTime PX: Comprehensive power analysis extension, vector-free analysis, NLDM/NLPM or CCS modeling
- VCS: SystemVerilog for design and verification, coverage analysis, multi-language support, extensive VIP library

Design Flow Deployment

Extensive experience with advanced designs, expertise with Synopsys' Galaxy™ and Discovery™ platforms, and significant investment in building and maintaining leading-edge flows in our own design centers make Synopsys Professional Services uniquely capable of helping you optimize your design flow for the challenges of implementing and verifying even the most advanced ASICs.

Because we're Synopsys, we're continually monitoring new tool releases and applying their most advanced features to our leading customers' design flows. And since Synopsys co-developed the reference flows for many of the leading IP providers and foundries such as ARM®, TSMC®, IBM®, Chartered®, UMC®, SMIC® and Common Platform®, we are the natural choice to customize and deploy them into your production design environment.

Now, with the availability of the Synopsys' Lynx Design System, you can deploy a complete, tapeout-proven RTL-to-GDSII flow that helps you addresses both design- and project-related bottlenecks. Our consultants are experienced users of Lynx, and can help you accelerate its deployment or customize it as necessary to meet the unique your unique design environment requirements.

Whether you're at the beginning or in the middle of your design project, whether you need a minor upgrade to your flow or a complete production-ready design system to migrate to a new nanometer design node, Synopsys Professional Services will help you eliminate the bottlenecks that impact your design productivity.

Synopsys' Design Flow Deployment services include assistance with:

- Assessment of your existing design flow and environment
- Implementation of production-ready sub-flows for project-specific challenges (e.g., timing, SI, low power, design-for-test)
- Deployment of complete design flows to ease ASIC-to-COT or new technology node (e.g., 90 nm, 65 nm, 45/40 nm, 32 nm, 28 nm) migrations
- Instantiation of customer-specific implementation methodologies (e.g., hierarchical or "virtual flat" design)
- Incorporation of new verification methods (such as assertions, functional coverage, and testbench automation) into existing environment
- Deployment and customization of the Lynx Design System (Production Flow and/or Foundry-Ready System) for customer-specific design environments, methodologies and process nodes
- Validation of new a new flow or sub-flow with a "pipe-cleaner" design and/or test chip

SoC Design and Verification

Synopsys consultants can work directly with your system architects to ensure the design specifications accurately capture design intent at both the block and chip levels, helping to minimize the iterations between the architecture and RTL implementation. We can then assist your team in translating the spec into a high-quality RTL description following best practices pioneered by Synopsys, as well as help identify suitable IP blocks and configurations to meet design goals.

By helping you employ the best design practices and the latest design methodologies in the front-end of the design cycle, Synopsys Professional Services enables you to achieve significant gains in overall design and verification productivity throughout the entire design process, and improve the predictability of your project schedule.

Synopsys' SoC Design and Verification Consulting services include assistance with:

- Design Feasibility
  - Analyze power, performance, area, complexity, design effort, risks, etc.
  - Vendor-neutral assessment of technology options
- Specification development
  - Capture and analysis of your design requirements
  - Creation of functional specification based on requirements
  - Identification of suitable IP blocks and definition of IP configuration
  - IC architecture development (block architecture, interfaces, etc.)
- RTL coding and verification
  - Translation of specification into RTL description
  - Early use of design and coding guideline checker (LEDA) to detect potential RTL issues
- Developing a robust verification plan
  - Translation of specification into golden model and testbench
  - Architecting layered, automated testbenches
- Deploying advanced verification methodologies for
  - Constructing bus functional models with both drivers and monitors
  - Developing and integrating verification IP
  - Generating constrained random stimulus
  - Automating functional coverage collection to fine tune random stimulus
  - Measuring and analyzing functional coverage
  - Deploying SystemVerilog assertions (SVA) or OpenVera assertions (OVA)

Rapid Prototyping

Synopsys' Confirma™ Rapid Prototyping solution provides a tightly integrated and comprehensive rapid prototyping flow for at-speed verification of FPGAs and ASICs. Synopsys' rapid prototyping software and hardware are ideal for IP and SoC design and verification teams who want to take advantage of advanced FPGA devices to quickly prototype their ASIC.

Synopsys consultants provide the expertise in methodology and implementation to help deploy a rapid prototyping flow that can efficiently map your ASIC-targeted RTL to Synopsys' HAPS™ or CHIPit™ hardware. Our engineers work collaboratively with your design team to define the flow and assist with the prototype implementation. The focus is to create a robust, reusable prototyping flow which puts your SoC design into actual hardware and enables "real world" testing and software integration in advance of ASIC availability.

Synopsys' Rapid Prototyping services include assistance with:

- Developing your prototyping methodology
- Test environment development and integration assistance
- Adapting your ASIC-targeted RTL for FPGA(s) (e.g., migrating memories, clocks, 3rd party IP)
- Configuring HAPS or CHIPit hardware (e.g., mapping standard interfaces and connectivity)
- Optimizing your rapid prototyping flow setup for RTL debug
- Configuring hardware for your verification strategy

Low Power Optimization and Verification

With expertise in low power tools and techniques, Synopsys consultants can help you manage your chip's dynamic and leakage power consumption. We will help you understand the inherent tradeoffs in using power-related technologies such as voltage islands, power and clock gating, multi-voltage design, dynamic voltage scaling, multiple threshhold voltages, MTCMOS and UPF/IEEE1801. With project requirements in mind, our consultants can then assist you in deploying the latest low-power techniques throughout the entire design flow, from synthesis, to functional verification and clock tree synthesis, through implementation and post-route optimization.

Synopsys' Low Power Optimization and Verification services include assistance with:

- Low power optimization and implementation
  - Assess current low-power techniques and methodologies including design intent, power constraints and scripts review
  - Recommend and deploy new low-power methodology including appropriate use of advanced low-power standards and techniques (IEEE 1801, DVFS, voltage islands, etc).
  - Develop new scripts and integrate them for project use
  - Develop low power test plan

- Low power verification
  - Customize low power verification test plan to guide simulation and coverage
  - Verify low power constructs such as isolation, power switches, and register retention
  - Verify protection cells added by synthesis, such as isolation cells, level-shifters, and retention registers
  - Verify implementation of power network added during place-and-route
  - Ensure UPF description is matched

Predictable Silicon Signoff

Our consultants can provide the methods and expertise to help you evolve a traditional ASIC handoff into an efficient, "hybrid-ASIC" handoff. A hybrid-ASIC flow can eliminate expensive iterations between front-end and back-end teams by incorporating physical implementation tools and analysis techniques earlier in the flow (e.g., during the physical synthesis step). The resulting physically-aware netlists incorporate design intent, floorplan data, utilization and congestion optimization for a more efficient handoff to the physical implementation team.

Synopsys' Predictable Silicon Signoff services include assistance with:

- Incorporating physical information early in the design cycle
  - New and complex library characteristics
  - Multi-voltage thresholds and multiple voltage domains
  - Multiple PVT corners, operating mode constraints, and clocks
  - Floorplan constraints
  - New physical requirements such as minimum double-via requirements
  - New test and verification strategies such as hierarchical scan
- Producing physically-aware netlists which take into account
  - Congestion
  - Incorporated low power techniques, special cells
  - Cell utilization
  - Special ASIC vendor requirements

Design Implementation Collaboration

Through hundreds of projects and more than 15 years of working with our customers on their most challenging chip designs, Synopsys Professional Services has established a leading-edge design competency, with consultants skilled in the latest EDA technology and design practices. Synopsys consultants utilize world-class tools from Synopsys' Galaxy Implementation Platform , a production-proven infrastructure including the Lynx Design System and extensive design experience to augment your project team. We deliver project support from the earliest phases of implementation through tape-out, identifying and resolving bottlenecks and transferring methodology and best practices throughout the engagement. From block level optimization to full chip integration, from IP integration and constraints management to power optimization and chip finishing, Synopsys experts can help you optimize your design's performance and accelerate your project schedules.

Synopsys' Design Implementation Collaboration services include assistance with:

- Hierarchical budgeting and design planning
- SI-aware place & route
- Full-chip timing/SI closure, static timing analysis and signoff
- Qualifying libraries, existing RTL and design constraints
- Generating and optimizing clock trees
- Power planning and optimization
- Full-chip extraction and in-design physical verification
- Chip finishing to tapeout
- Support for netlist, placed-gates, or GDSII manufacturing handoffs as well as concept-to-parts
- Adopting demonstrated methods and baseline scripts for follow-on project use

System-Level Modeling Services

Synopsys has an extensive and successful track record of collaborating with customers to create and deploy transaction-level models (TLMs) and virtual platforms for their early software development. With more than 150 staff-years of engineering experience in building models and platforms, this proven experience and expertise in both hardware and embedded software design will help you achieve your system-level modeling goals.

Our experts provide the following services to your project teams:

Model Creation

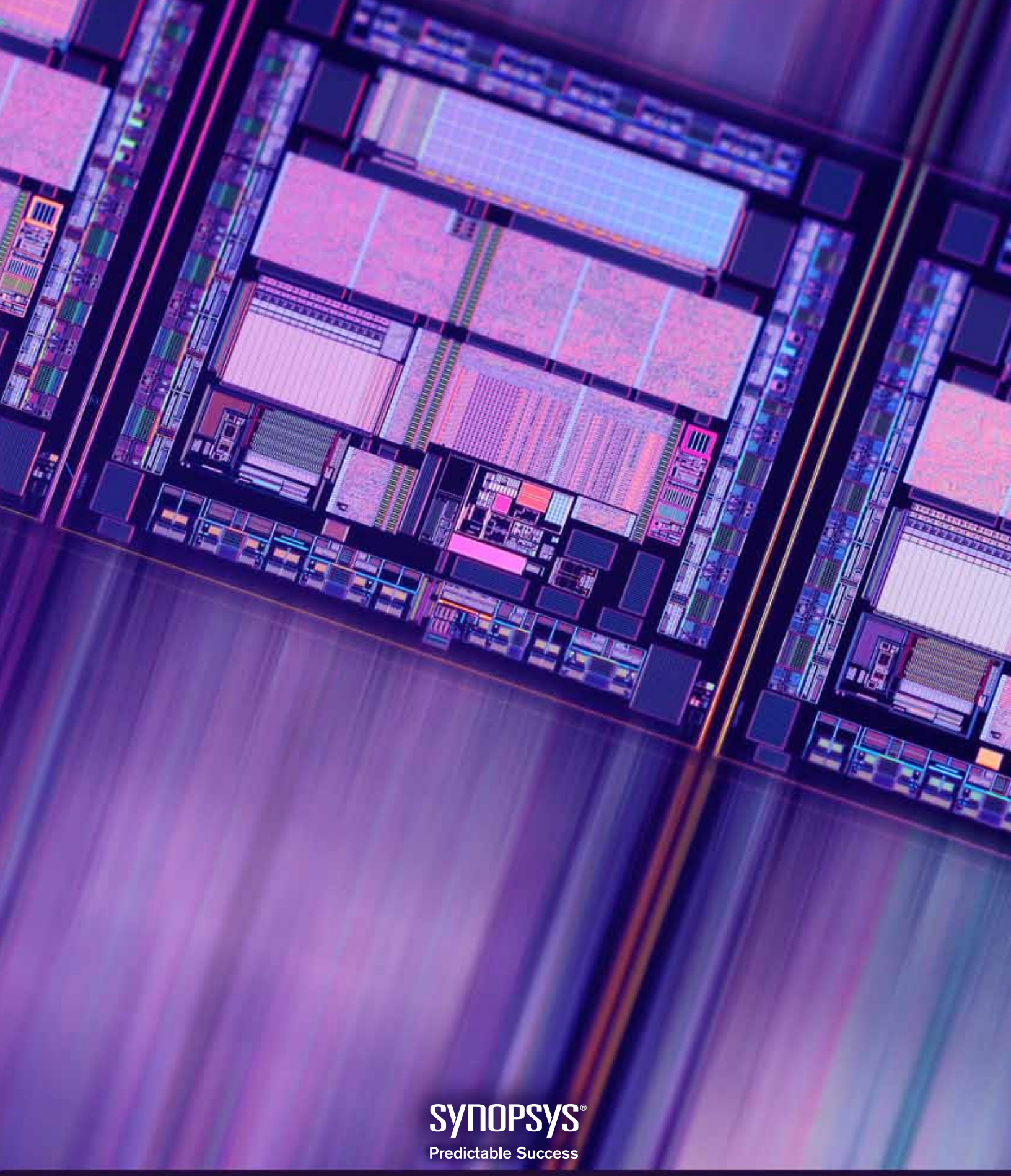
The development of new or customer-specific transaction-level models not currently available in the DesignWare® System-Level Library is a key ingredient of delivering high-performance, customized virtual platforms. Our focus is on speed and accuracy: the models are built for fast simulation execution with accurate representation of the hardware so that the same software that runs on the models runs on the hardware – unmodified.

Virtual Platform Assembly/Customization

Synopsys will assist with the assembly of TLMs into a new virtual platform representing your specific embedded system, or the customization of a pre-existing platform to represent the latest design intent. Virtual platforms are more than a collection of models; their creation requires system-level understanding and knowledge of tools for developing and executing virtual platforms, such as Synopsys' Innovator and CoMET. With over 100 complex virtual platforms developed to date, Synopsys is uniquely qualified to help you integrate, debug, and test your virtual platform while we transfer knowledge to your team.

System-Level Methodology Consulting

Synopsys experts deliver consulting and training on virtual platform tools and methodologies to accelerate your team's learning curve and system-level modeling productivity.



SYNOPSYS®

Predictable Success

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