

Synopsys and Ricoh

Processor Designer's Automated Flow Enabled Ricoh to Quickly Develop a Custom DSP for Office Automation Products



Processor Designer provided exactly what we needed—an easy way to create a high quality custom DSP letting us focus on our design expertise rather than RTL and software toolchain implementation details.”

RICOH**Sadahiro Kimura**

Senior R&D Engineer, Core Technology R&D Center, Ricoh

Business

Ricoh offers innovative approaches and solutions to accommodate advanced contemporary information requirements in imaging solutions, industrial products, and other key areas.

Challenges

- ▶ Needed to redevelop an outdated custom DSP but lacked the time and experience to do the development in-house

System-Level Design Solution

- ▶ Processor Designer custom processor design tool

Benefits

- ▶ Automated custom processor development process
- ▶ Ease of use despite lack of custom DSP development experience
- ▶ Ease of processor description using LISA language enabled continuous refinement & enhancement of the processor to meet project needs

Overview

The Core Technology Research and Development (R&D) team at Ricoh is responsible for creating and testing new and differentiated technologies for Ricoh's various product lines.

The R&D team needed to develop an application-specific digital signal processor (DSP) for office automation products, such as copiers and printers, using a custom instruction set. Although a custom DSP had been created by R&D in the past, the team no longer had the RTL code or debugger tool. They also did not have much direct experience with DSP development.

Leading Custom Processor Design Solution

Since creating the new DSP with a manual RTL design approach would have cost the team considerable time and engineering effort, they choose to use Processor Designer.

Processor Designer automated the design process generating both a software development tool flow and RTL. Input for the design was all done in the LISA language. Ricoh quickly got up to speed and found that using LISA produced a high level of

design productivity. For example, a specific ALU block consisted of 1,531 lines of LISA code. The generated RTL code had 10,006 lines, an almost 7x abstraction. The final DSP gate count was 29,464 gates including scan logic for testing and runs at 200 MHz.

The overall result was fast time-to-results with low engineering effort while meeting performance goals based on the defined custom instruction set. Ricoh plans to continue using Processor Designer for this type of project.



Predictable Success Synopsys, Inc. • 700 East Middlefield Road • Mountain View, CA 94043 • www.synopsys.com

©2011 Synopsys, Inc. All rights reserved. Synopsys is a trademark of Synopsys, Inc. in the United States and other countries. A list of Synopsys trademarks is available at <http://www.synopsys.com/copyright.html>. All other names mentioned herein are trademarks or registered trademarks of their respective owners.

05/11.AP.CS623.