

# Synopsys and CEVA

## CEVA's MM3000 Mobile Multimedia Platform Successfully Used Processor Designer for 2 Advanced DSP Designs



*For an advanced and innovative design like the MM3000, Processor Designer was the only tool that offered the needed tool flow integration and flexibility to get to the optimum implementation.”*

**Erez Bar-Niv**  
CTO, CEVA

### Business

CEVA is a leading licensor of silicon intellectual property (SIP) platform solutions and DSP cores for mobile handset, consumer electronics and storage application. CEVA's IP portfolio includes comprehensive solutions for wireless baseband, multimedia, audio, voice over packet (VoP), Bluetooth and Serial ATA (SATA), and more.

### Challenges

- ▶ Need to meet tight market window and still have flexibility for innovative multicore design
- ▶ Shorten cycle time while optimizing feature tradeoffs
- ▶ Create integrated tool flow to speed iterations

### Design Solution

- ▶ Processor Designer custom processor design tool

### Benefits

- ▶ Offers most integrated tool flow enabling the best optimizations for performance and area
- ▶ Generates optimized RTL for quick implementation on both FPGA and ASIC
- ▶ Fast debug with integrated debugger

### Overview

CEVA's latest mobile multimedia platform digital signal processor (DSP) IP is the MM3000. This multipurpose, programmable high-definition (HD) video and image processing platform utilizes a heterogeneous, multicore architecture. The core of the platform consists of two specialized processors—a Stream Processor and a Vector Processor, both designed using Synopsys' Process Designer tool.

The Stream Processor is responsible for bit stream coding, bit stream manipulation, and control code execution, while the Vector Processor performs filtering and vector operations typical for pixel processing. There are multi-instances of both processors in the platform.

The MM3000 comes complete with C compilers and power management provision intended to be able to process any and all video codecs up to the highest resolutions and frame rates currently available as well as future codecs for things like 3-D video. The architecture is specifically constructed to enable: augmented reality, gesture recognition, face detection and recognition, facial expressions recognition and object detection as well as full image pipeline and other ISP functionality.



*Synopsys' global R&D and field support teams were key to completing such an innovative design in a short time-to-market window."*

**Erez Bar-Niv**  
CTO, CEVA

### **Leading Custom Processor Design Solution**

The MM3000 design team needed a tool that allowed for a large amount of flexibility, handling many iterations while helping shorten cycle times to get to market faster. This innovative design contains one DSP at around 600K gates and another at around 1.1 million gates scaling to 40nm, 28nm or other process nodes, and supports ISP functionality (pre-processing and post-processing) as well as multiple standards (H.264 HP, VCI, Real Video, AVS, VP6/7/8 and future standards such as Scalable Video Codec (SVC) and Multi-view Video Codec (MVC)), so the design project required a custom processor tool capable of fast turnaround on iterations and a tight integration of the software tool chain.

Processor Designer automatically generated key software development tools like a debugger, assembler and linker and quickly generated optimized RTL for design implementation. CEVA's team quickly came up to speed using Processor Designer's LISA input language.

With Processor Designer's RTL generator, the team quickly ported the multicore processor designs to FPGAs. They were able to run AVC and MVC HD streams in real-time, a testament to the design team's expertise and the tool's seamless tool chain flow from C to RTL.

Unlike other tools or more traditional manual methods, Processor Designer offered CEVA's team the best integration of a software tool chain, RTL generation and SW debugger speeding design iterations and allowing the exploration needed to find the optimum implementation. The result is a scalable architecture so the number of stream and vector processors in addition to the type and size of the memories can be configured to address each specific use-case. Additionally, each processor is configurable and can be upscaled and downscaled.

### **High-Quality Global Support**

Because of the level of innovation required to design the MM3000, CEVA took advantage of Synopsys' global R&D and field application engineer support teams. The MM3000 design project took Processor Designer's capabilities to the extreme. Through this collaboration, the Synopsys R&D team expanded the tool's features and became better prepared to handle advanced processor design.

When released, CEVA's MM3000 can be used as a video processing engine for every high-definition application, from smart phones, via computers to games consoles and digital televisions.

*"With Processor Designer, we were able to quickly port the design and run AVC and MVC HD streams in real-time on FPGAs—a major accomplishment."*

**Erez Bar-Niv**  
CTO, CEVA



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