

Synopsys and STMicroelectronics

Rapid Delivery of Demodulator IP for Analog TV Standards using Symphony Model Compiler High-Level Synthesis Solution



By using Synopsys' Symphony Model Compiler we were able to complete our entire validation effort within two weeks and with extremely reliable results."

Srevats Laxman

Technical Leader IP Algorithms, STMicroelectronics



Business

STMicroelectronics is a global semiconductor company producing a variety of devices, ranging from single transistors to microprocessors and complex SoCs. The ST Bangalore site focuses on the design of algorithmic IP cores for ASICs that are used in digital TVs and consumer multimedia products.

Challenges

- ▶ Improve productivity of multirate TV demodulator algorithms for ASIC implementation
- ▶ Reliably implement and verify algorithm in standard RTL ASIC flow
- ▶ Reduce length of complex verification process due to multirate algorithm requirements
- ▶ Avoid delays in tape-out
- ▶ Achieve 3X faster turnarounds for real-time FPGA verification

System-Level Design Solution

- ▶ Synopsys Symphony Model Compiler (SMC) high-level synthesis tool, ASIC Edition

Benefits

- ▶ Fast ramp up and ease-of-use with SMC high-level IP model library
- ▶ Rich IP set including DDS, FFT, multirate filter banks, CORDIC
- ▶ 5X greater high-level exploration capability of multirate HW architecture tradeoffs
- ▶ Fast implementation into RTL using high-level synthesis (HLS)
- ▶ Complete verification and validation in 2 wks vs. multiple months using other design flows
- ▶ MATLAB-driven verification
- ▶ Easy and reliable ECO flow for incremental change in ASIC flow, eliminating tape-out delays

Overview

This ST team works on multi-standard digital TV demodulators that support worldwide TV broadcasting formats (digital and analog). Implementation of these demodulators using advanced Digital Signal Processing (DSP) algorithms enables integration into low cost ASICs. These algorithms require complex multirate processing and, for better performance, need to be implemented in direct silicon circuits rather than DSP cores or CPUs.

In the past, direct implementation of these algorithms in an ASIC (or FPGA) has been a challenge because of the complexity of mapping them accurately and reliably into the RTL of the ASIC or FPGA flow. In particular, the management of multiple sample rates and the associated choices in HW architecture, multiple clock domains and reliably implementing clock-domain crossings (CDCs) is time consuming and error prone.

Rapid Algorithm Design and Exploration

ST used Symphony Model Compiler to create their demodulator IP algorithms for analog TV standards in a high-level, model-based design environment. This environment, based on Simulink from MathWorks®, provides IP model libraries, multirate management, vector arithmetic and other features that allow rapid design capture and verification of a fixed-point multirate algorithm.

In addition, the ST design supports low-IF architecture for channel bandwidths between 6 and 8 MHz, a requirement to meet all worldwide standards. It uses Hilbert filtering and decimation and includes two PLLs and six mixed-signal AGC controls to drive the front end. It also performs audio/video separation and audio rate conversion. The processing chain used an intermediate frequency input sampled at around 160 MHz, three digital mixers, two PLLs and 10 filters including four down sampling converters.

A key benefit of SMC is the ability to describe and verify the multirate and mixed-signal behavior of the algorithm very quickly and very early in the project timeline, and then use the SMC HLS engine to create optimized RTL for ASIC and FPGA flows.

High-Level Synthesis of Multirate Algorithms

ST used the SMC HLS engine to create the ASIC implementation and FPGA prototype of the TV demodulator algorithm. This eliminated coding and verification efforts by easily translating design intent into high quality-of-results RTL for use in standard ASIC and FPGA RTL flows using Synopsys Design Compiler and Synplify® Premier.

Furthermore, ST was able to quickly explore various HW architecture tradeoffs to optimize the design. Because SMC is tightly coupled with Design Compiler and Synplify Premier, its HLS optimizations such as pipelining/retiming, folding and IP micro-architectural selection, are more accurate, thus reducing timing closure.

Reliable ASIC and ECO Flow Integration

ST has successfully taped out their latest demodulator core in a 65-nm ASIC. The team also evaluated the ECO capabilities by trying simple changes in the design, and realizing metal-only changes in the output without re-running the whole flow. This raised the confidence in the SMC-ASIC flow and the team is now moving on to the next IP design project using SMC. “Because of the ability to easily re-target, re-optimize, and re-verify with SMC, we plan to reuse this TV demodulator core across many advanced ASIC technology nodes from 65-nm and smaller,” said Srevats Laxman, Technical Leader, IP Algorithms, STMicroelectronics.

“Symphony Model Compiler let us rapidly evaluate different hardware architectures of our demodulator algorithms, and also make small ECOs quickly and reliably. This cut months off our schedule and significantly reduced risk in our IP and ASIC development projects.

Gurudatta Mewundi
IP Manager, STMicroelectronics

