SYNOPSYS®

DATASHEET

Lynx Design System

Delivering Higher Productivity and Predictability in IC Design

The Lynx Design System is a full-chip design environment that includes innovative automation and reporting capabilities to help designers implement and monitor their designs

Overview

Lynx Design System includes a baseline RTL-to-GDSII flow that can be leveraged to simplify and automate flows for many critical implementation and validation tasks, enabling engineers to focus on achieving performance and design goals. Developed by chip designers for chip designers, the Lynx Design System is based on tools from the industry-leading Galaxy™ Design Platform, and has been validated with more than 100 tape-outs from 180-nanometer (nm) to 7-nm.

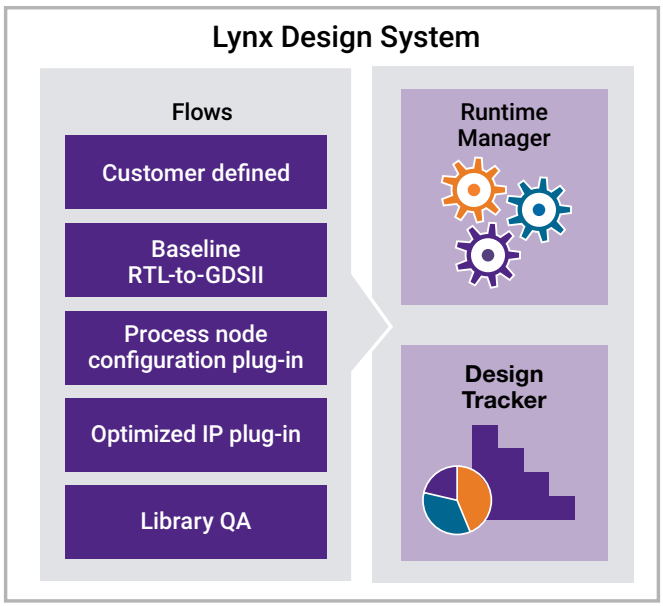

Figure 1: The Lynx Design System

User Benefits

- Visualization technology provides intuitive, easy-to-use flow creation, execution automation and project reporting
- Build innovative and sophisticated automation solutions such as circuit validation, correlation and IP regression to improve productivity
- Production-proven design flow incorporates the latest methodologies to deliver fast and predictable results
- Open environment provides library and foundry independence with support for 3rd party tools, enabling flow portability and customization across multiple projects
- Technology plug-ins enable foundry and library data configuration and validation, reducing risk and accelerating project schedules

Runtime Manager

The Lynx Design System includes a patented GUI (Figure 2) that simplifies and automates flow creation, configuration and maintenance to improve the productivity of the design team. Intuitive and easy-to-use, Lynx's Runtime Manager provides the ability to graphically edit, execute and monitor customer flows as a design progresses from RTL to tape-out. Creating a new design flow or modifying existing flows is accomplished using intuitive edit operations. Flat or hierarchical design flows, for a single block or for an entire chip, are defined by connecting various tasks together based on their execution dependencies. Parallel task execution, design exploration involving multiple runs of the same task or experimenting with different parameters in the design flow are also easily accomplished within Lynx's Runtime Manager.

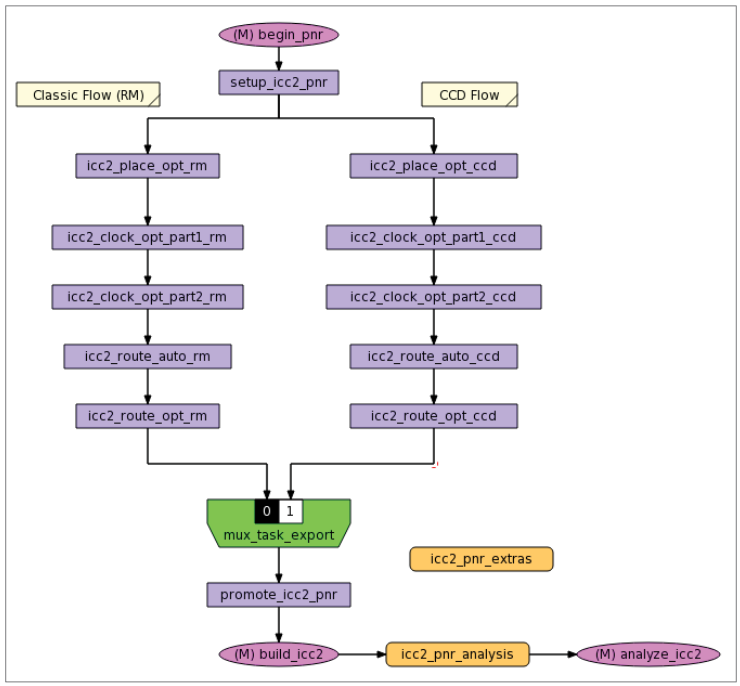

Figure 2: Patented GUI enables easy creation, configuration and debug of design flows at multiple levels

Included with Runtime Manager is a distributed high performance computing (HPC) workload management optimization feature called Adaptive Resource Optimizer (ARO). ARO (Figure 3) monitors usage patterns of submitted jobs and determines a more optimal value to be used for reserving compute resources (e.g. memory, CPUs) of future job submissions based on historical use data.

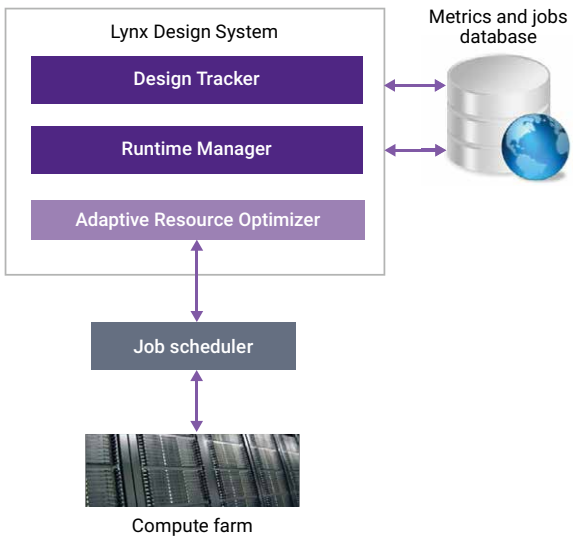

Figure 3: Adaptive Resource Analyzer

ARO can substantially reduce job pending time, the time a job sits in queue waiting for a resource, and improve compute resource utilization by ensuring that jobs are assigned to the best queue/machine combination. The busier the HPC environment, the greater the benefit realized from ARO compared to traditional fixed resource management practices. Improvements of 10% or more in each job's turnaround time, the time it takes from job submission to getting results, can be achieved using ARO. When aggregated across thousands of jobs, ARO significantly improves the productivity of the design team.

ARO currently supports LSF, SGE and UGE, but can be adapted for proprietary environments as well.

Design Tracker

The Lynx Design System provides designers and managers with 'on-demand' access to many design and system metrics. Flow metrics can be design related, task related or process related and can be easily extended to include user-defined metrics based on the task being executed. Users can create status and trend reports such as quality-of-results (QoR) and resource-related project metrics. Metrics can automatically be captured during flow execution and stored for customized reporting capability.

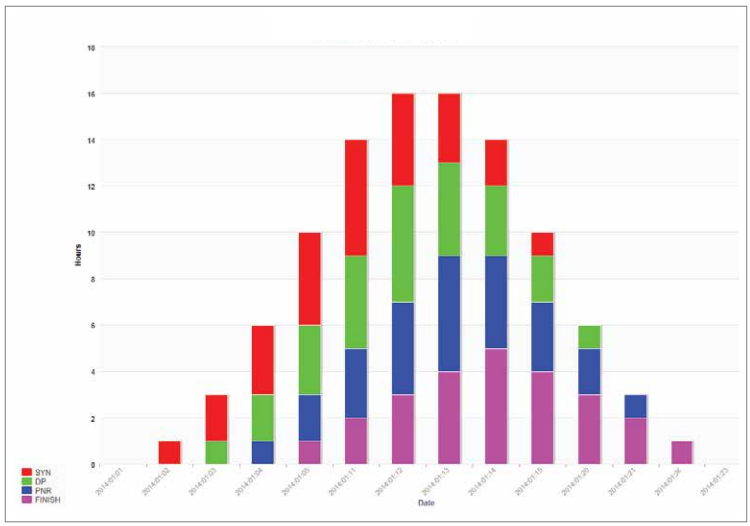

Figure 4: Report of time spent at each design step facilitates analysis of design bottlenecks

Lineage		Progress		Content				Timing					
								Setup			Hold		
Design Name	Snapshot	Progress Step	Progress Dst	Area	Utilization	Cell Count	Flop Count	Setup NVP	Setup TNS	Setup WNS	Hold NVP	Hold TNS	Hold WNS
dhm	2015_02_22	30_pnr	icc_clock_opt_psyn	9336	30	9670	1138	0	0.00	0.00	1	0.00	0.00
dtop	2015_02_22	20_dp	icc_commit	22303	63	10164	4573	0	0.00	0.00	285	11.87	0.13
dhm_upf	2015_02_22	30_pnr	icc_initial_route	12243	19	10853	1151	0	0.00	0.00	14	0.03	0.00
dtop_upf	2015_02_22	20_dp	icc_power_insertion	44898	51	40511	4628	81	22.85	0.62	3119	23714.91	11.43
dhm_ram	2015_02_22	30_pnr	icc_clock_opt_cts	35095	67	24612	1932	0	0.00	0.00	117	2.05	0.05

Figure 5: Instant "Dashboard" snapshot of the most important design metrics, comparing actuals to targets at various steps in the design flow

The powerful visualization capabilities in Design Tracker converts a simple CSV-like text file called a "Lynx DT" file into tables (with colorization and hyperlinks to source data), plots and bar graphs like those shown in the Figures 4 through 7. Design Tracker includes sample report generation scripts for the RTL-to-GDSII flow. Customized scripts can be easily created to parse important information from logs and reports, write the information in Lynx DT format, and view the output with Design Tracker.

In addition to Lynx DT files, Design Tracker provides an interface for sharing any web-viewable content securely among project members, including hand-generated HTML, text files, images (PNG, JPG and GIF) and PDFs.

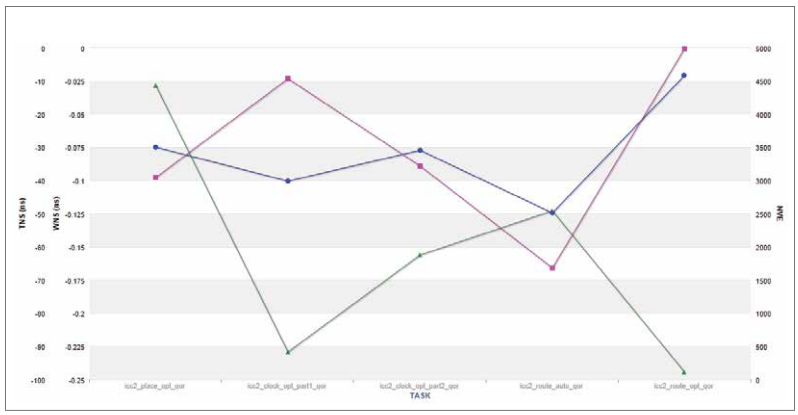

Figure 6: WNS and TNS trend across design flow steps

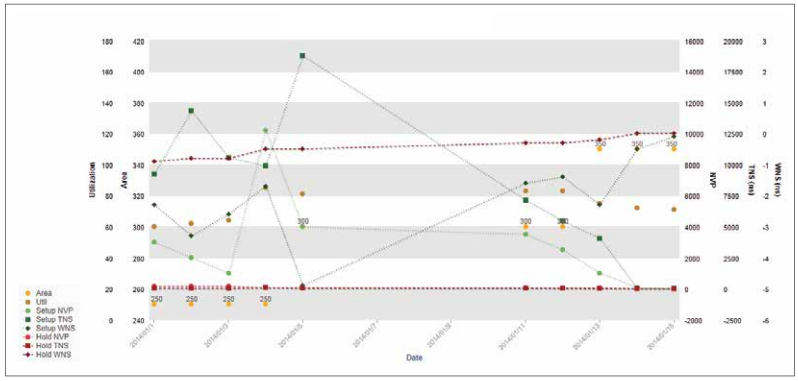

Figure 7: Various metric trends over time

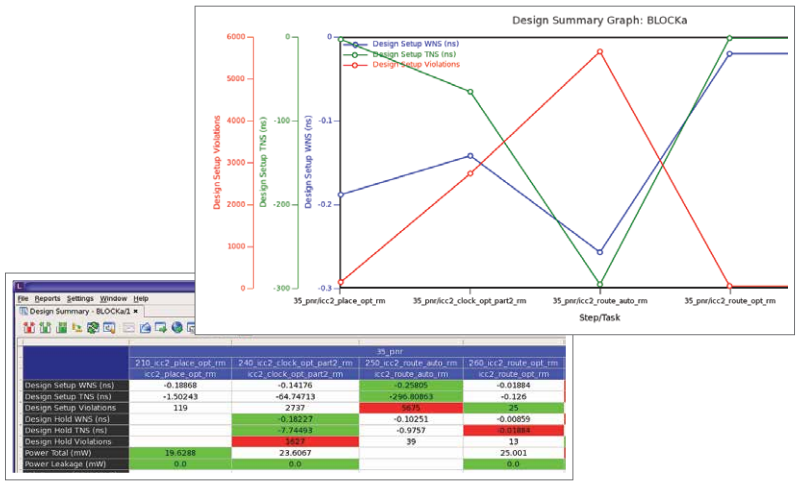

Figure 8: Immediate access to design and flow metrics

Design Tracker also includes a “QoR Viewer” that gives designers immediate access to design and flow metrics as interactive reports (Figure 8) from the Runtime Manager, enabling data-driven and faster decisions. Through these interactive reports, designers can analyze design metrics ranging from runtime and tool memory usage for each tool and task in a flow, multi-corner multi-mode (MCMM) timing and power data for each timing path in the design. All reports can be plotted as line or bar graphs and dashboards with coloring rules. These reports can be exported as images or comma-separated value (CSV) files for post-processing.

The QoR viewer accelerates collaboration between designers with features that enable designers to compare current runs against previous experiments or experiments performed by other members of the project team. Designers can share their report setups as specification files that can be used by others.

The QoR Viewer is architected to be extensible and customizable. Designers, design teams and CAD organizations can modify the content and format of existing reports and create their own reports that show data of interest for a specific task or project.

Flow

The Lynx Design System can be leveraged to create and automate flows for many critical implementation, validation, regression and correlation tasks, enabling engineers to focus on achieving project goals. The comprehensive environment includes:

- Production ready RTL-to-GDSII flow
- Technology process node configuration plug-in
- Optimized processor and interface IP plug-ins
- Library quality assurance (QA) flow

The baseline RTL-to-GDSII flow is tuned to deliver superior quality of results with the Synopsys Galaxy Design Platform. It allows designers to customize tool capabilities and methodologies based on their specific project needs and integrate third-party tools as needed. For example, designers can configure Synopsys tools such as Design Compiler® Ultra, Design Compiler Graphical, TetraMAX® ATPG, PrimeTime®, IC Compiler, IC Compiler II, IC Validator, StarRC™, VC CDC and VC LP, Galaxy Custom Router™, HSPICE® and NanoTime. This hierarchical, baseline RTL-to-GDSII implementation flow includes the following features:

- Synopsys Galaxy Design Platform reference methodologies
- Built-in methodologies for design optimization, including optimizations for low power, area, performance and manufacturability
- Full-chip hierarchical RTL-to-GDSII support
- Validation with multiple standard cell libraries and foundry technology nodes
- Design environment support for job distribution, job submission optimization, revision control and data management
- Project-based deployment model enabling multi-site and multi-user support
- Full technical support and regular updates to the latest tools and methodologies

While the Lynx baseline flow is tuned to deliver superior quality of results with the Synopsys Galaxy Design Platform, you can readily incorporate other Synopsys or third-party tools into the design flow by updating standard and well understood TCL scripts.

The technology process node configuration, optimized processor and interface IP plug-ins, along with Library QA flow, are pre-validated scripts and utilities that help accelerate project start and reduce the time it takes to get to optimized design results.

Lynx's process node configuration plug-in gives designers a template configuration of tool and flow settings to quickly configure the Lynx flow for their choice of standard cell libraries and memories. To further expedite project setup, pre-validated configurations for commonly-used libraries and process nodes are optionally available. They include process technology information and representative flow and tool settings for specific libraries and foundry nodes spanning from 180-nm down to 7-nm.

Processor cores are often the most critical IP block in a SoC, and optimizing the implementation for the best balance of performance, power and area can require a significant amount of effort. To provide design teams with a more productive starting point, Lynx's optimized processor and interface IP plug-ins include pre-tuned and IP-specific flow scripts, optimized timing and DFT constraints, floorplans and placement guidance, IP-specific tool settings, design and floorplan exploration and comparative analysis flows for leading processor cores and interface IP, including:

- Arm® Cortex™-A7 MPCore
- Arm Cortex-A15 MPCore
- Arm Cortex-A17 MPCore
- Arm Cortex-A53 MPCore
- Imagination Technologies PowerVR™ Series6 GPU Core
- Synopsys ARC® HS34, HS36 and HS38 processors
- Synopsys DesignWare® DDR4, DDR3 and PCI Express® Interface IP

The processor and interface IP specific flows encapsulate the best design practices for optimization and hardening of processor cores and interface IP, shortening design team time to optimized performance, power and area results in chosen process technology.

Mismatched, incorrect, or incomplete technology and library files can negatively impact a design project's schedule and a designer's productivity. The risk is especially high at newer process nodes where technology data is constantly changing. The library quality assurance plug-in includes scripts and documentation to configure and pre-test any library and technology files for proper execution in the design flow. These comprehensive data and integration checks help ensure that the incoming library and hard IP are configured correctly in the context of the design.

For more information on Synopsys Lynx Design System please visit www.synopsys.com/lynx

SYNOPSYS®
Silicon to Software™

©2018 Synopsys, Inc. All rights reserved. Synopsys is a trademark of Synopsys, Inc. in the United States and other countries. A list of Synopsys trademarks is available at synopsys.com/copyright.html. All other names mentioned herein are trademarks or registered trademarks of their respective owners.
09/14/18.CS270036585_Lynx DS.