Synphony Model Compiler
High-Level Synthesis for Model-Based Design

Faster and More Efficient Hardware Development from Model-Based Design
Model-based design environments are popular for algorithm design and exploration because they allow concise representations of behavior at very high levels of abstraction. These environments provide fast design capture and more productive simulation and debugging tools. However, problems arise when the designer needs to translate the design intent into RTL hardware (HW) for ASIC or FPGA implementation tools. Hand-coding RTL of these algorithms proves to be very time consuming and prone to error because of re-coding and re-verification into the RTL domain. Furthermore, HW architecture exploration is limited because of these difficulties. The Synphony Model Compiler solution addresses these problems by providing an easy and automated way to synthesize ASIC and FPGA hardware from high-level models created in the Simulink/MATLAB model-based environment.

High-Level IP Model Library
Synphony Model™ Compiler (SMC) provides a comprehensive, high-level model library for creating math, signal processing, and communications designs in the Simulink environment. The library makes it very easy to capture fixed-point, multi-rate algorithms and optimize/debug their precision. Most blocks in the SMC library support up to 128-bit precision, floating-point override, and overflow, min/max logging capabilities, which enable rapid exploration of word lengths, quantization, distortion, and other algorithmic performance tradeoffs. The SMC library also supports vector notation which enables quick and concise capture of large multichannel or highly parallel algorithms.

Figure 1: Synphony Model Compiler provides a faster, more automated path from high level algorithm descriptions to FPGA or ASIC, prototypes and verification flows.
Hardware Optimizations, Exploration, and Verification using High-Level Synthesis

Using a verified SMC model, the SMC high-level synthesis (HLS) engine creates RTL for hardware implementation and enables rapid exploration of architecture tradeoffs using HLS optimization technology. This not only achieves higher design productivity but also reduces errors and risk by maintaining consistent verification across multiple architecture choices and target technologies. Given a user-specified FPGA or ASIC target and some architecture directives/constraints, the HLS engine automatically optimizes at multiple levels by applying pipelining, scheduling, and other architecture optimizations across the entire system, including IP blocks and throughout design hierarchy. The SMC HLS engine also includes advanced technology characterizations that utilize the Synopsys Synplify® Premier or Design Compiler® implementation products to make device-specific optimizations for the FPGA or ASIC target respectively; thus achieving better results across technologies and providing tighter timing correlation through the RTL implementation flow. This methodology also increases the reliability of verification through these design project phases, regardless of whether the target is for FPGA-based prototyping, fast architecture exploration, or ASIC implementation.

C-Output for Faster System Modeling and Earlier System Validation

Developing ASIC and FPGA hardware blocks often requires a significant system-level integration, simulation and validation effort. Synphony Model Compiler significantly improves the productivity of system validation by automatically creating C-based models of the HLS RTL output. This eliminates the difficult and time consuming effort of creating models by hand. SMC C-model generation is very flexible by creating high performance, fixed-point ANSI-C models that can be used in a variety of system simulation environments including Simulink, SystemC, and RTL simulators like Synopsys' VCS® functional verification solution and Mentor Graphics' ModelSim. Synphony Model Compiler brings these capabilities together for the first time in a single environment that supports complete, integrated solutions with Synopsys' FPGA implementation, ASIC implementation, prototyping, and verification flows.

Improve Time-to-Market and Reliability

Synphony Model Compiler can shorten algorithm HW design cycles by as much as 70%, especially when real-time FPGA-based prototyping and technology portability are required. Design teams can validate algorithm concepts earlier in the design cycle, catch functional and system level problems earlier, and explore design space tradeoffs more rapidly. With a more automated flow from higher levels of abstraction, system and algorithm designers can achieve higher productivity, reliability and time-to-market in their ASIC and FPGA projects.

For more information about Synphony Model Compiler, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.
<table>
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<th>Features</th>
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| Synthesizable fixed-point, high-level IP model library | - Broad set of signal processing functions for wireless and communications  
- Multi-rate support                             
- Vector support for fast creation of large multichannel or parallel algorithms  
- Up to 128-bit precision (most blocks)         
- Fixed-point analysis and debugging support (min/max and overflow logging)  
- Synthesizable and optimizable by high-level synthesis implementation flow |
| Multi-rate algorithm design                   | - Broad high level multi-rate library support                            
- High level synthesis optimizations across multiple sample rates             
- Clock circuit generation and management of clocking strategies             |
| RTL encapsulation support                    | - Use RTL within your high-level SMC model                               
- High performance simulation with no external RTL simulators required        
- Easily add state machines, control logic, and cycle-accurate interfaces to your high-level SMC model  
- Easily use 3rd party IP in your high-level SMC model                        |
| High-level synthesis optimizations and transformations | - Automatic system-wide retiming/pipelining at the architecture level  
- Automatic folding/scheduling for area optimization                          
- Automatic IP-level micro architecture optimizations                        
- Target-aware optimizations for FPGAs and ASICs                               |
| HLS subsystems                               | - Partition designs into a hierarchy of HLS-optimizable subsystems        
- Verify top-level designs using high-level simulation and debugging         
- Independently apply and tune HLS optimizations for different subsystems    
- Scale the HLS flow for larger designs with higher quality of results       |
| ASIC flow integration                        | - Automatic generation of RTL constraints and scripts for Design Compiler  
- Advanced timing estimation using Design Compiler                              
- Rapid architecture exploration of speed, area and power tradeoffs          |
| FPGA flow integration                        | - Automatic generation of RTL constraints and scripts for Synplify Pro/Synplify Premier  
- Advanced timing estimation using Synplify Pro®/Synplify Premier            
- Optimized resource mapping to advanced FPGA devices such as hardware multipliers, MACS, adders, memories and shift registers |
| RTL testbench generation                     | - Automatic generation of text vectors and scripts for RTL verification in VCS |
| C-model generation                           | - C-model creation for fast system-level validation and simulation        
- Cycle-accurate with the post-optimized RTL output                           
- High performance simulation: over 100X faster than RTL simulation           
- Automatic wrapper generation for various simulators: Simulink, VCS, ModelSim, and generic ANSI-C direct executable |