Solutions for DO-254

Overview

- Industry-leading functional verification
- Widely adopted circuit verification
- Production-proven equivalence and static checking
- Market-leading FPGA synthesis and debugging
- Unique solutions for FPGA-based prototyping of ASIC, ASSP and SoC designs
- Fast time-to-verified RTL using model-based high-level synthesis

Overview

The purpose of RTCA/DO-254, recognized in 2005 by the FAA, is to ensure safety in airborne electronic systems. As the standard means of compliance for ASIC, FPGA and PLDs used in such systems, DO-254 is composed of five levels of stringency, levels A to E, that are based on the effect of the failure of the hardware upon an aircraft. Meeting Level A compliance requires a much higher level of validation and verification than would Level E compliance. DO-254 provides the necessary process guidelines to ensure the design’s requirements are met, and ensure the highest quality in all safety-critical designs destined for use in aircraft.

DO-254 Compliance

DO-254 compliance dictates a requirements-based design and verification strategy that would include designing strictly to the definition of requirements and performing accurate, complete and independent verification of the design against these requirements. Synopsys offers a comprehensive suite of solutions that address the needs of DO-254 compliant ASIC and FPGA development and verification.

Verification

Accurate functional verification versus initial requirements is a critical component of meeting DO-254 standards. A Synopsys verification flow based on the VCS® RTL verification solution coupled with Universal Verification Methodology (UVM) techniques, promotes the creation, execution and measurement of a complete verification environment. Synopsys supports the generation of an executable verification plan linked to requirement documents with automatic back annotation of metric results to aid in the management and closure of verification goals required by DO-254. Additionally, Synopsys provides powerful solutions for static checking, formal analysis, logical, sequential and functional equivalency, giving designers’ confidence in developing multiple, and functionally equivalent design views.

FPGA Synthesis

Every year, a growing number of safety-critical designs are implemented in FPGAs. It is important to have a proven and reliable solution for transforming an idea into programmable logic from any vendor. Synopsys offers the Synplify® family of high-performance, technology-independent implementation and debugging solutions designed to aid DO-254 compliant processes for FPGA development.
FPGA-Based Prototyping

Prototyping can be an important step in verifying DO-254 compliance. Synopsys’ HAPS® family of FPGA-based prototyping solutions provides an integrated and scalable hardware-software solution for hardware-based validation of ASIC and FPGA-based systems. Together, our suite of tightly integrated and easy-to-use HAPS hardware plus software tools dramatically accelerate software development, hardware/software integration and system validation.

Functional & Formal Verification – verifying and tracking function vs. requirement

VCS, the industry’s most comprehensive RTL verification solution, provides a wide range of features that help to verify an ASIC or FPGA design against safety critical requirements. These include advanced bug-finding technologies (e.g. SystemVerilog, complete assertions, and comprehensive code and functional coverage) and support for the reusable verification techniques of the widely adopted UVM.

Verification Planner and the Unified Report Generator, used in conjunction with VCS and the Verdi debug platform, provide a coverage analysis and reporting environment that further aids DO-254 compliance by providing easy tracking of functional coverage, verification progress vs. requirements and compatibility with widely used requirements capture practices.

VC Formal technology also supports unreachable analysis to ensure that coverage goals are correct. Such coverage analysis can help achieve the 100% coverage required for DO-254 compliance.

Circuit Simulation & Verification – verify that your design will behave as expected

Saber® is a key component of a robust design methodology in DO-254 compliant flows. A full featured simulation environment for mechatronic designs, it provides transient, frequency, statistical, and functional safety analysis capabilities, a large library of component models and templates across numerous physical domains, as well as report generation in standard formats necessary to meet DO-254 traceability requirements.

HSPICE® is the IC industry’s “gold standard” for accurate circuit simulation and offers founcry-certified MOS device models with state-of-the-art simulation and analysis algorithms. HSPICE is a highly accurate circuit simulator that precisely predicts circuit timing, power consumption, functionality and yield, as well as accurate signal and power integrity simulation of high-speed interconnects between chips and PC boards that are necessary in meeting DO-254 requirements.

FineSim™ is a high-performance circuit simulator that accelerates simulation of complex analog/mixed-signal circuits with SPICE accuracy. FineSim’s unique multi-core/multi-machine (MCM) simulation capability enables users to drastically improve simulation performance and capacity. FineSim is well-suited for simulation of large, complex analog circuits to meet the requirements of DO-254.

CustomSim™ is a FastSPICE simulator that delivers the superior performance and capacity necessary to verify post-layout effects of complex circuits, including custom digital, memory and analog/mixed-signal. The CustomSim solution includes advanced analysis options for native circuit ERC checking, power, signal and MOS reliability analysis, enabling you to verify your designs with confidence of DO-254 compliance.

The VCS® AMS mixed-signal verification solution delivers industry-best performance and capacity for faster mixed-signal SoC simulation and regression testing. VCS AMS enables the rapid development of a coverage-driven, constrained-random testbench that can be run in parallel across compute farms to verify your designs with confidence of DO-254 compliance.

Equivalence & Static Checking – assure that your design views are in sync

Formality® is a logical equivalence-checking solution that uses formal techniques to verify that the pre-synthesis design (RTL) is logically (Boolean) equivalent to the post-synthesis design (netlist), without the use of test vectors. HECTOR is a functional equivalency checking solution to verify that a high-level design description (C/C++/SystemC) is functionally equivalent to an RTL implementation on a transaction-accurate basis. VC Formal's sequential equivalency checking capability is a functional equivalency checking solution to verify that a RTL description is functionally equivalent to an RTL implementation after some transformation (power gating insertion, for example) on a cycle-accurate basis. Formality, HECTOR and VC Formal support all major hardware description languages and database formats to provide the most comprehensive functional equivalence checking solution available.

ESP-CV is a functional equivalence checker for comparing a design in progress with a reference design. These designs may be described as Verilog behavioral models, RTL, UDPS, gates, transistors, or SPICE netlist views. Formality and ESP provide fast and complete functional coverage, enabling you to quickly find bugs and establish functional equivalence.

VC CDC is a Clock Domain Crossing (CDC) static checking solution. VC CDC works at the RTL to identify any type or variant of CDC synchronizer use, finding synchronization bugs at any level of the design hierarchy, from block-level to full-chip flat. VC CDC offers the performance and capacity to load and run enormous designs at full-chip flat, and provides the highest accuracy with the lowest violation reporting noise.

LEDA® is a programmable design and coding guideline checker. It enables DO-254 compliant design reuse with prepackaged guidelines, such as the Reuse Methodology Manual (RMM), and verifies consistency of design and SDC constraints between synthesis and physical verification.
**FPGA Synthesis – ensure safety-critical programmable logic**

Synopsys’ proven development process and widely used design tools can help you to meet your requirements without compromising safety or performance. Synopsys’ Synplify family of design and implementation tools enable you to develop a reproducible requirements-driven design process that includes system specification, RTL coding, logic synthesis and verification. The Synplify Premier product offers safety-critical capabilities for SEU mitigation such as automation of triple modular redundancy, fault-tolerant FSM implementation and automatic inference of error correcting memory. Designers use Synopsys’ FPGA design and verification tools for implementation of DO-254 processes to meet FAA standards and ensure the safety of airborne hardware.

**FPGA-Based Prototyping – validate your design well ahead of chip fabrication**

Synopsys provides the most complete portfolio of FPGA-based prototyping systems and software tools, HAPS, HAPS-DX and ProtoCompiler to accelerate software development, ease hardware/software integration and speed system validation (e.g., co-simulation, transaction-based validation and links to virtual prototyping). HAPS and HAPS-DX systems are based on a modular architecture and design flow, which are ideal for accelerating the creation of proof-of-concept prototypes. Together, our suite of tightly integrated and easy-to-use hardware plus software tools dramatically accelerates functional validation of ASIC, ASSP and SoC designs.

**Model-Based High-Level Synthesis – save months from concept to verified hardware**

With Symphony™ Model Compiler (SMC), design teams can create and verify FPGA and ASIC hardware from high-level modeling environments such as Simulink®. The SMC IP model library enables teams to manage their DO-254 verification requirements from a much higher-level of abstraction and increase the reliability, scope and speed of their verification suites. The SMC high-level synthesis (HLS) engine generates optimized hardware, RTL testbenches, and a high-performance C-model for system-level simulation. Symphony Model Compiler is the only HLS tool in the industry that creates hardware accurate C-models of its optimized RTL. Using this model-based high-level synthesis methodology, system and hardware engineers can achieve over 10X verification productivity while drastically cutting the time it takes to create verified, reliable hardware.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.