SYNOPSYS®
Predictable Success

Solutions for DO-254

At-a-Glance

- *Industry-leading functional verification*
- *Widely adopted circuit verification*
- *Production-proven equivalence checking*
- *Market-leading FPGA synthesis and debugging*
- *Unique solutions for Rapid Prototyping of ASIC/FPGAs*

Overview

The purpose of RTCA/DO-254, recognized in 2005 by the FAA, is to ensure safety in airborne electronic systems. As the standard means of compliance for ASIC, FPGA and PLDs used in such systems, DO-254 is composed of five levels of stringency, levels A to E, that are based on the effect of the failure of the hardware upon an aircraft. Meeting Level A compliance requires a much higher level of validation and verification than would Level E compliance. DO-254 provides the necessary process guidelines to eliminate functional errors and ensure the highest of quality in all safety-critical designs destined for use in aircraft.

Requirements

DO-254 compliance dictates a requirements-based design and verification strategy. This strategy would take into account the definition of requirements, designing strictly to those requirements, and performing accurate, complete and independent verification of that design. Synopsys offers a comprehensive suite of solutions that address the needs of DO-254 compliant ASIC and FPGA development and verification.

Verification

Accurate functional verification versus initial requirements is a critical component of meeting DO-254 standards. A Synopsys verification flow, centered about the VCS® RTL verification solution coupled with the VMM methodology, promote the creation, execution and measurement of a complete verification plan. Additionally, Synopsys provides powerful solutions for checking circuit, formal and functional equivalency, giving designers' confidence in developing multiple, functionally equivalent design views.

FPGA Synthesis

Every year, a growing number of safety-critical designs are implemented in FPGAs. It is important, then, to have a proven and reliable solution for transforming an idea into programmable logic from any vendor.

Synopsys offers the Synplify® family of high-performance, technology-independent implementation and debugging solutions designed to aid DO-254 compliant processes for FPGA development.

Rapid Prototyping

Prototyping can be an important step in verifying DO-254 compliance. Synopsys provides Confirma™, a unique portfolio of applications and tools that enable hardware-based verification for both ASIC and FPGA based systems. These tightly integrated, easy to use products facilitate complete system debugging and early software development.

Functional & Formal Verification – verifying and tracking function vs. requirement!

VCS, the industry's most comprehensive RTL verification solution, provides a wide range of features that can help you verify an ASIC or FPGA design vs. safety critical requirements. These include advanced bug-finding technologies (e.g. native testbench, complete assertions, and comprehensive code and functional coverage), and support for the reusable verification techniques of the widely adopted Verification Methodology manual (VMM).

VMM Planner and Unified Report Generator, used in conjunction with VCS, provide a coverage analysis and reporting environment that further aids DO-254 compliance by providing easy tracking of functional coverage, verification progress vs. requirements and compatibility with widely used requirements capture practices.

Magellan™, an RTL formal verification solution, utilizes VCS to find deep corner case bugs in complex designs, while reducing "false negative" errors, Such added coverage can help achieve the 100% coverage required for DO-254 compliance.

Circuit Simulation & Verification – verify that your design will behave as expected!

The Saber® simulator is a key component of a Robust Design methodology in DO-254 compliant flows. A full featured simulation environment for mechatronic designs, it provides transient, frequency, and statistical analysis capabilities, a large library of component models and templates across numerous physical domains, and report generation in standard formats necessary to meet DO-254 traceability requirements.

CustomSim™ is a high capacity, transistor level simulation solution that can efficiently verify different classes of circuits, including custom digital, analog and memory. Using the simulation technologies of NanoSim® and XA, CustomSim helps you verify the consistency of transistor level representations of large digital circuits vs. their RTL/gate level counterparts, allowing you to design and simulate with multiple views of a circuit with confidence of DO-254 compliance.

Equivalence Checking – assure that your designs view are in sync!

Formality® is an equivalence-checking solution that uses formal, static techniques to verify that multiple versions of a design are functionally equivalent, without the use of test vectors. Formality supports all major hardware description languages, database formats, to provide the most comprehensive verification solution available.

ESP-CV is a functional equivalence checker designed for comparing a design in progress with a reference design; designs may be described as Verilog behavioral models, RTL, UDP's, gates, transistors, or SPICE netlist views. It provides fast and complete functional coverage, enabling you to quickly find bugs and establish functional equivalence.

LEDA® is a programmable design and coding guideline checker that finds complex bugs, such as those associated with multiple clock domains using static analysis. It enables DO-254 compliant design reuse with prepackaged guidelines, such as the Reuse Methodology Manual (RMM), and verifies consistency of design and SDC constraints between synthesis and physical verification.

FPGA Synthesis – ensure safety-critical programmable logic!

The Synplify family of products provide the ultimate FPGA implementation and debug environment for advanced FPGA design and ASIC/ASSP verification using FPGA-based prototypes. This solution offers hardware designers a comprehensive suite of technology-independent tools that address the most challenging aspects of today's FPGA design including timing closure, logic verification, debug, reliability, IP usage, ASIC compatibility, DSP implementation, and tight integration with FPGA vendor software.

Rapid Prototyping – accelerate verification at the board level!

The Confirma platform is a complete suite of tightly integrated, easy to use products for rapid prototyping including FPGA-based prototyping systems and boards, interface and memory boards, and implementation and debug software. It is ideal for design and verification teams who leverage FPGA-based prototypes to find and eliminate those "hardest-to-find" hardware bugs that could compromise the predictability and safety of an airborne system.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.

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