



# FORUM

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# YIELD ANALYSIS AND OPTIMIZATION ENSURES TIGHT DESIGN-TO-MANUFACTURING LINKS

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As chip technology grows ever more sophisticated, new materials and manufacturing techniques create yield challenges that were unimagined in the early days of the IC. Effective production of semiconductors at very deep-submicron geometries thus requires maintaining a careful balance between design and manufacturing. Problems once considered the sole domain of one or the other now require solutions that tighten connections between the two while minimizing yield loss.

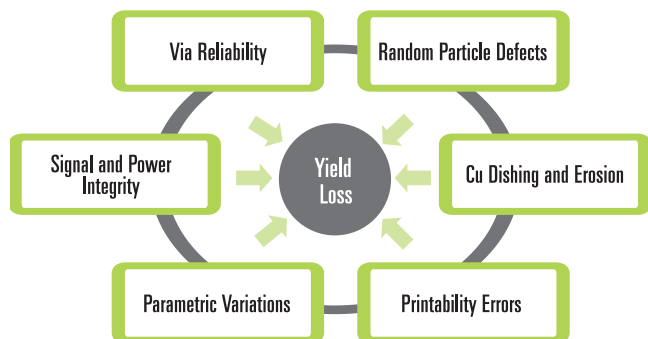
Today, foundries, as well as mask and lithography vendors, recognize the importance of fostering relationships with providers of design-for-manufacturing (DFM) solutions. Specifically, manufacturing-aware design tools that provide accurate yield analysis and optimization capabilities are critical to addressing leading-edge production requirements.

## EVOLUTION OF YIELD CHALLENGES

With the advent of the 130-nanometer device generation, new materials, such as copper, began to be utilized to boost interconnect speed, while low-k dielectrics, such as SiLK, were employed to improve resistance/capacitance (RC) delays, power dissipation and reduction of metal levels. At the same time, chipmakers began to implement optical proximity correction (OPC), phase-shifting masks (PSMs) and other resolution enhancement techniques (RETs) to extend the life of their existing lithography tools. Unfortunately, introducing all of these new materials and techniques at once drastically reduced final product yields.

Today, the industry is experiencing an unprecedented increase in complexity and, accordingly, in yield loss mechanisms (Figure 1).

**Figure 1. Many Interrelated Problems Can Degrade Yield**



*Advanced technology nodes and new materials have combined to increase the sources of defects that can negatively impact device yields.*

As classical CMOS scaling approaches its practical limits, the further introduction of new materials is generating unique processing challenges associated with etch and deposition chemistries. Moreover, systematic and parametric defects, as well as random defects, are now recognized as culprits that contribute to yield loss. This means that products must emerge from technology development with high yields, and then ramp quickly to entitled yield.

Entitled yield is a well-known manufacturing term, referring to the fact that as a process matures, the achievable yield will improve to its optimal level – the entitled yield. Therefore, an integrated solution that anticipates yield issues during the design phase is required to ensure a smooth transfer to manufacturing. Effective DFM solutions must span the entire design-to-silicon flow and use best-in-class capabilities. With this approach, manufacturing costs can be controlled, and chipmakers have a much better chance of meeting their greatly tightened market windows.

## FINDING AND ADDRESSING SOURCES OF YIELD LOSS

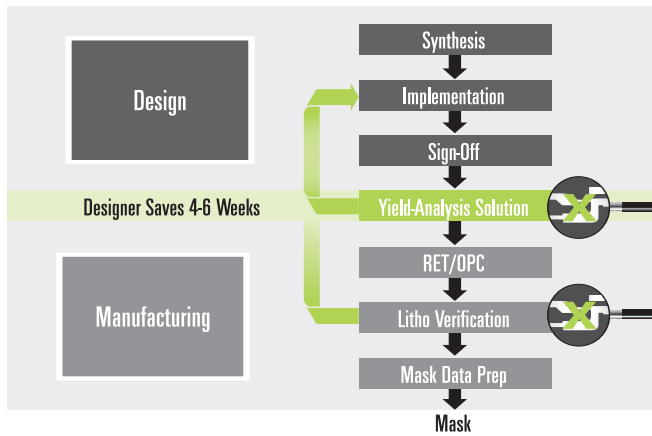
As the industry moves toward 65- and 45-nanometer technology nodes, the most pressing manufacturing challenges center on variations produced by lithography and chemical mechanical polishing (CMP) processes and by random particle defects that crop up throughout device production. The key is to translate these challenges into a language that designers can understand, allowing them to create structures that are tolerant and improve yield.

Previously, DFM analysis and repair was treated with a rules-based approach. Following a set of minimum and recommended rules provided by the foundry, design engineers would craft their designs using a “best guess” approach based on their own experience and judgment. Models representing true process behavior were unavailable, severely limiting the degree to which designers could accurately analyze yield issues. As a result, more and more systematic failures were occurring, with no way for designers to clearly identify and correct design issues, given the limitations of the process.

A unified yield analysis approach, on the other hand, takes a comprehensive approach to DFM, consisting of tools that work together to bring manufacturing data to the design process, enabling identification of critical yield issues and providing correction guidance. Lithography, CMP and random defects/particles – the most pervasive sources of first-order yield loss – are highly interdependent, so resolving design challenges associated

with one area can create a new problem in another. An integrated yield analysis and optimization solution avoids this “ping-pong” effect by treating these critical yield issues in an all-inclusive manner. Tight links to design implementation provide further control for the designer as well (Figure 2).

**Figure 2. Accelerating Time-to-Yield**



*A truly integrated yield-analysis solution comprising a suite of process-centric capabilities is critical to accelerating time-to-yield.*

Especially critical is the employment of production-baseline technology and manufacturing models used by leading foundries and integrated device manufacturers (IDMs). Incorporating real, rather than simulated, encrypted foundry production data allows tools to understand the process that will be used to manufacture the design while protecting the foundry’s critical intellectual property (IP). This enables designers and manufacturers to exchange data in a way that makes sense to both of them, allowing them to speak each other’s language without having to learn each other’s job.

Currently, due to the lack of manufacturing-aware design analysis tools, issues related to design are identified well after the OPC/RET implementation is complete. Problems are flagged at the lithography verification step to check manufacturing suitability. As a result, the design must go back to the place-and-route stage, thus causing several weeks of delay in addition to lost revenue.

Different process steps pose unique challenges. For example, CMP must be carefully controlled to prevent overpolishing. Similarly, the lithography process raises printability issues at geometries that are smaller than the wavelength of light, meaning that the designer’s intended structure may not be what ends up printed on silicon. Manufacturing issues can also arise from variations in temperature, mechanical equipment vibrations, etc. that occur during production. Generally, these types of problems are difficult to model deterministically, calling for a probabilistic approach. It’s essential to understand these issues and the potential variations, and then address them where possible during the design phase.

#### **Lithographic Sensitivities**

Accurately patterning a design layout onto a wafer is more difficult today than ever before, thanks to the delayed development and deployment of advanced lithography equipment needed to print the microscopic features of a 65-nanometer chip. The current generation of 193-nanometer lithography equipment is now being extended to 65- and 45-nanometer technology nodes by immersion lithography. This combination of nanometer technology node and lithography equipment, with only a fraction of the necessary resolution, results in extremely poor printability. Even with RET

approaches, design patterns often experience distortions at some process conditions, changing the electrical behavior of the circuit. The result is greater variability, leading to parametric yield loss.

Once a hotspot is identified, it must be corrected to prevent a catastrophic design failure or to reduce excess variation and increase parametric yield. In the case of interconnect correction, close cooperation between the analysis tool and the routing tool is required to intelligently correct potential hotspots in a reasonable time within the normal router flow. Working in the background, the analysis tool seamlessly finds, prioritizes and fixes hotspots within the normal router flow, coupling real-time analysis and correction to create higher yielding silicon.

#### **Poor Wafer Planarization**

At the 130-nanometer process node, a major shift occurred when many semiconductor companies switched from aluminum to copper as their metal interconnect of choice. In the aluminum process used for previous process nodes, metal is deposited and then etched to create the interconnect lines. An additional deposition of inter-layer dielectric (ILD) is used to isolate interconnect lines, followed by a planarization step. In the copper process, however, the pattern for the metal traces is etched into the ILD, and copper is electroplated into newly created trenches. The excess copper material is removed in a CMP step, so variations in wafer height may appear in areas where metal density is not uniform, creating erosion or ditching, depending on whether too much or not enough copper material is removed. This can result in electrical variations within the device.

Like the lithographic effects mentioned earlier, variations due to poor planarization result in additional parametric yield loss. These variations manifest themselves as increased variability in timing due to increased resistance in interconnects. Excess timing variations may affect the ultimate operating frequency of the chip or even, ultimately, destroy the functionality of the chip.

To correct for planarity issues, rule-based metal fill is a common approach for inserting dummy metal fill to achieve uniform metal distribution and adequate planarization. A design rule check (DRC) tool is used to apply the fill, driven by a set of CMP design rules to constrain the fill algorithm. More complex fill strategies may incorporate a library of fill patterns with different sizes and shapes. Simple fill algorithms may apply the metal insertion in a single pass; more complicated algorithms begin with larger patterns and apply smaller and smaller patterns in subsequent passes. However, a fundamental limitation of this technique is that timing impact is not considered. As a result, the metal fill may aid wafer planarity at the expense of circuit timing.

Rather than introduce an additional correction step that may compromise the timing of the circuit, the best approach is to employ correction within the normal router flow. The yield analysis solution works seamlessly in the background, advising the router on an optimal fill strategy while the router performs timing-driven metal fill. The analysis tool can also be used in a stand-alone manner to separately validate the design for the existence of planarity issues. Using this approach safeguards design timing while creating a design with the best possible planarity.

#### **Random Particle Defects**

Yield loss due to random particle defects has been understood for many process generations. During semiconductor processing, random particles can attach to the wafer surface and cause an unintended short circuit between two design elements, creating a bridge fault and destroying the function of the chip. In the same manner, a defect can also sever a physical net in the circuit, preventing the device from functioning correctly by

creating an open circuit condition. When either the critical area or the defect density inherent in the process increases, the probability of a good device decreases, thus lowering yield.

Random particle defects can destroy circuit function by creating an unintended bridge or break condition in the layout pattern. The yield analysis tool performs a critical area analysis on the design to predict the possibility of these manufacturing faults. This analysis determines a particular layout's sensitivity to random particle defects, given different defect sizes are likely to be found in the process. Using critical area information, together with defect density data for different defect sizes, predicted yield loss due to random particle defects can be calculated.

An additional challenge is that multiple fabs impose additional design constraints, so designs must not only be robust within a specific range of process windows and variability parameters, but must also be able to accommodate various fab processes as well. Although some design differences are inevitable to accommodate different processes, they need to be minimized as part of the focus on comprehensive DFM.

All of this underscores the need for sophisticated DFM capabilities that can work reliably in the face of incomplete process technology data, as well as access and utilize exact process models and DFM flows from individual fabs/foundries. Since the inception of DFM, software has moved from point tools to complete tool suites to fully integrated solutions that

can address a host of design- and process-induced challenges. To be effective today and remain effective going forward, DFM solutions must be able to consistently acquire, analyze and share critical information throughout the design-to-silicon flow. This enables the elimination of systematic yield challenges at the design level, expanding the process window and, ultimately, enabling highly accurate yield prediction and optimization for chipmakers, fabs and foundries. ■

#### ***About the Author***

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