Introduction
The consumer’s insatiable demand for greater performance, a shrinking form factor and extended battery life, all while continuing the trend for lower end user cost is the driving force behind the semiconductor industry’s rapid evolution to ever smaller process geometries.

As with many of the previous process geometry shrinks, there will be the usual concerns about the increase in design complexity, the management of power consumption and the need to get products out in a timely fashion. However, while there are perceived capacity, power and performance benefits at this node, without careful consideration of the design tools, these benefits could easily be removed by the myriad pitfalls of over designing, unnecessary guard banding, poor manufacturing yield or simply taking too long to get the chips designed and hence missing that all-important market window of opportunity. The large increase in cost for designing these IC’s will limit adoption in the early years to the highest volume applications where competition for the lowest cost, highest performance AND lowest power is fierce, and the potential cost of failure is enormous.

For the first time, the significant impact of manufacturing techniques required for 20nm and the sheer size and complexity of the geometries involved will have a dramatic impact on every aspect of the EDA tool chain and the related design/CAD flows currently in use. Therefore, an ever closer interaction between these tools is needed to ensure that the overall product goals can be met. To manage the risk and ensure success at this node, tighter collaboration with leading EDA vendors will be paramount, and the ramifications of not aligning to the optimum flow will be numerous.

Many early adopters are already partnering with Synopsys to leverage emerging capabilities and the close interoperability found throughout the Galaxy™ Implementation Platform of tools. This new node compared with 28nm, promises a doubling of logic densities while delivering a significant 30% improvement in performance or 25% lower power at the same operating frequencies.

This white paper will highlight the major challenges of building ICs at the 20-nm node, will hopefully help you identify the tool and design flow changes required and ultimately show you how the Synopsys Galaxy Implementation Platform meets and exceeds these new challenges.
Challenges

Without a doubt, 20nm is considered an extremely complex technology to produce with many more design rules, more electrical variations and other factors to consider. In addition to this, 20nm introduces new manufacturing challenges such as double patterning which is needed for finer pitch patterns than would be possible using current lithography techniques. This is especially true with the current immersion lithography wafer processing that utilizes a wavelength of 193nm, and the lack of Extreme Ultra Violet (EUV) technologies to address the diminishing contrast and thus resolution of these shrinking nodes.

Double patterning lithography uses two masks to print closely spaced patterns. It splits layers that do not meet the minimum spacing requirements on to two separate masks (constituting the two colors). The exposures from the masks are overlaid to print the desired single layer with the finer pitch.

Figure 1: Double patterning technology

At 20nm, double patterning technology (DPT) using two masks is expected. However, at more advanced nodes, such as 14nm and below, the industry is anticipating three, possibly four patterns per layer. Until EUV can deliver on its promise, DPT will be the required route for designing at finer geometries. This technique enables the track pitches to be manufactured much closer together, decomposing the required layer image into two patterns that can be exposed separately. By exposing the patterns separately this allows the spacing or pitch of the structures to be reduced by a factor of two (or more for triple/quadruple patterning). Figure 1 above shows an example of double patterning at work.

Figure 2: Double patterning technology decomposition

Unlike previous process nodes, the impact of double patterning cannot be isolated to steps late in the design flow; this technique of splitting up the mask efficiently and effectively is complex and important for ensuring the complex spacing rules can be met. This requires DPT-compliant library preparation and knowledge of the rules much earlier in the flow where cell selection and placement is a critical factor. For example, Figure 2 shows how a mask could be decomposed for metal tracks in a preferred direction.
However, routing patterns are not guaranteed to conform to the same orientation. As shown in Figure 3, a redundant via array can introduce orthogonal layout patterns, which can cause double patterning spacing violations in the decomposed mask. This double patterning spacing conflict in a mask could be fixed/resolved by applying a split-and-stitch technique as shown in Figure 4. A polygon, which is split into two pieces and decomposed to separate masks, is stitched together during manufacturing.

Compared to a conventional printed layout as shown in Figure 5, a stitched layout could suffer from printability degradation due to complex line-end effects. These potential degradations need to be considered early in the design flow to minimize their effect on performance, manufacturing yield or reliability. The design flow can support pre-coloring of sensitive or critical nets to avoid this impact if desired.
To ensure a manufacturable product, there is a significant increase in the number of rules over previous technology generations and at 20nm this stands at over 5,000 rules. Examples of these new rules the router needs to be aware of and adhere to are shown below in Figure 6.

Allied to the potential degradation in the manufactured structures is the variation in the parasitics within and between these manufactured geometries. This results in a significant source of variability between what is expected during implementation and what is eventually patterned. A critical issue is the impact on timing variations caused by this misalignment affecting both the final performance, as well as the timing validity of the circuit. These spacing and/or geometric changes to the resultant structures impact the parasitic capacitances, resistances and even inductances. These changes need to be modeled accurately and the information made available to both the implementation and sign-off tools. An example of these types of variations can be seen below in Figure 7 graphically in (a) and the impact on capacitance in (b).

Besides all complexities introduced by using multiple patterns, device aging represents another key challenge in 20-nm integrated circuits. Device aging is mainly due to the degradation of the gate dielectric and of the interface between gate dielectric and silicon over time. Two important mechanisms that contribute to such degradation are the Hot Carrier Injection (HCI) and the Bias Temperature Instability (BTI). These mechanisms are more prominent in the 20-nm process because the gate dielectric is scaled to only a few atoms in equivalent thickness. Device aging increases the threshold voltage and decreases the channel carrier mobility which degrade circuit performance over time, shorten circuit lifetime and introduce potential failures in the field. Long and expensive testing is required to assess the degradation of circuit performance and failure in time (aging), thus increasing the overall manufacturing cost. Alternatively, designers may use conservative rules to overdesign the critical circuits, increasing the chip cost.
Critical Tools for 20nm

Manufacturers are anticipating that the 20-nm technology node will provide a halving of area over the 28-nm node. While many designers will benefit from much smaller and potentially lower cost IC’s, many others will attempt to push the technology to its limits and maximize the capabilities of their products. SOC’s with over 20 billion transistors will be possible and that will pose a giga-scale challenge for many of the EDA tools. A significant improvement in runtime, tighter tool-flow interoperability and a substantial increase in design capacity and concurrent analysis will be required to meet the productivity requirements to make designs of this size meet the continually aggressive product schedules. Further refinement and streamlining of design flows and design methodologies are also expected to deliver optimal turnaround times.

The Galaxy Implementation Platform comprises a comprehensive suite of tools to implement both standard cell-based and fully custom designs. Included in this platform is a number of best-in-class industry-leading tools including Design Compiler®, IC Compiler™, IC Validator, StarRC™, Primetime®, HSPICE® and Galaxy Custom Designer®. These tools provide a single, unified and productive environment for producing signoff-quality designs at all major process nodes and foundries including the emerging 20-nm technology node.

The 20-nm node introduces new challenges particularly in the area of transistor level changes and severely restrictive topology choices, new Middle-of-Line (MOL) local interconnections, an increase in complex design rules, layout dependent effects to name a few. Many of these will be transparent to most designers as the EDA industry develops viable solutions that provide productivity and minimal impact on every day design methodologies. Design sizes will be growing significantly at 20nm as designers leverage the available real estate they have to work with, add functionality and ultimately end-user value through the delivery of high levels of integration and features.

To improve the overall throughput of larger designs, Synopsys has recently introduced a number of new technologies and enhancements to their industry-leading design solutions, including wider use of multi-cpu processing Synopsys physical guidance (SPG), and signoff-driven ECO tools for example.

We will focus here on the areas that will have an unavoidable design impact:

- Modeling and Extraction
- Physical Verification
- Physical Implementation

Modeling and Extraction

A critical component in the EDA tool-chain is accurate modeling and extraction to reflect as closely as possible the parasitic effects and timing delays that can be expected in the final silicon. StarRC™ is the EDA industry’s gold standard for parasitic extraction. A key component of Synopsys’ Galaxy Implementation Platform, StarRC provides a silicon-accurate and high-performance extraction solution for SoC, custom digital, analog/mixed-signal (AMS) and memory IC designs. StarRC offers full-chip ScanBand and integrated Rapid3D fast field solver technology for proven sub-femtofarad accuracy.

![Figure 8: StarRC support](image)
As discussed previously, DPT enables the printability of narrowly spaced device and inter-connect layers in 20-nm IC manufacturing by splitting the layers into two separate masks. However, multiple exposures using two masks can introduce additional variability in both front-end-of-line (FEOL) as well as the back-end-of-line (BEOL) processing phases as a consequence of mask misalignment in the manufacturing process. The two masks can shift in both x and/or the y direction, causing spacing and hence coupling capacitance variation, that in turn can impact the circuit performance. The performance change on critical nets as a result of this misalignment can potentially be up to 15%, thus, accurate DPT variation modeling and parasitic extraction are critical requirements for designs at 20nm.

Synopsys’ StarRC parasitic extraction solution accurately accounts for the critical lateral capacitance variation due to mask shifts through silicon-calibrated models that correspond to additional process or RC (Resistance-Capacitance) extraction corners. Since the additional “DPT” corners mean more time-consuming extraction and STA runs, StarRC mitigates the impact through simultaneous multi-corner extraction and by generating a multi-value SPEF (Standard Parasitic Extraction Format) netlist that provides min and max capacitances for a net, based on spacing variation. Synopsys' PrimeTime static timing analysis and sign-off tool uses this multi-value SPEF to apply the appropriate capacitances in the same analysis run. Figure 9 illustrates StarRC’s modeling of the mask misalignment variation and the multi-valued SPEF link with PrimeTime for accurate analysis.

In addition to the mask shift variation modeling, StarRC also provides accurate capacitance extraction for any interconnect layers “pre-colored” (or pre-marked and constrained to be on same mask) by designers due to timing sensitivity. StarRC’s pattern-matching and 3D extraction technologies enable accurate extraction and signoff of standard or pre-colored designs.

All leading 20nm foundries have been working closely with Synopsys while developing the technology and have qualified StarRC for this technology node.

Physical Verification
Within the Galaxy Implementation Platform, physical verification is performed by IC Validator using foundry-proven signoff DRC runsets. IC Validator can check many design rules to validate the double patterning rules as well as the many additional manufacturing rules imposed by the foundries. This tool has been developed to analyze large areas of the chip and leveraging multi-cpu processing to help scale to large low geometry designs. Some of the additional requirements including timing aware dummy metal fill and pattern matching to detect structures in the design known to impact manufacturing yields. Synopsys has created a capability where problematic patterns identified by their TCAD process simulation tools or identified in the yield management tools used by the foundries can be provided to IC Validator to help quickly improve manufacturing yields.
IC Validator incorporates a comprehensive range of techniques using a combination of property and equation based techniques to check conformity to foundry rules. By incorporating IC Validator In-Design, it provides a unified environment where the designer can avoid the potentially huge time lost addressing issues like DPT rule violations detected late in the design process. While potentially many of the double patterning rules could be built into the place and route tools, the implementation tools may not be able to see conflicts or rule violations at a chip level or across hierarchical boundaries. Synopsys’ recommendation is to perform and fix physical violations at each step in the flow. IC Validator In-Design works natively with IC Compiler to ensure these checks with many complex rules can be made very quickly to converge on sign-off closure efficiently. Figure 10 shows how IC Validator In-Design would be used in an advanced geometry design like 20nm.

A new, native hierarchical DPT coloring engine in IC Validator enables fast DPT decomposition analysis. The coloring engine makes it possible to accurately detect and quickly resolve DPT color conflicts. In addition, IC Validator native coloring allows for a variety of stitching techniques per foundry requirements. Fast native coloring accelerates verification time and shortens debug for physical designers.

IC Validator In-Design has been foundry qualified and can also be used with both IC Compiler and Galaxy Custom Designer for physical verification of cell based and custom circuits. The resultant GDSII for the chip will not be colored, enabling the foundries to make the optimal final decomposition choices. IC Validator’s In-Design technology provides coloring information within the Milkyway database for parasitic extraction required for timing analysis and verification.

**Physical Implementation**

**Standard Cell**

Double patterning technology requires a place and route tool that accurately generates a layout where each candidate layer can be decomposed into dual alternating patterns without undue impact on performance and area. This requirement adds another complexity to the tools that, until now, have focused mainly on meeting timing area and power goals while incorporating some DFM (Design for Manufacture) requirements.

To avoid surprises during sign off and to maximize the benefits of this technology node, the implementation tools, IC Compiler and Custom Designer, within the Galaxy Implementation Platform are double pattern rule aware for most of the requirements, where needed the complex rules can be checked by IC Validator In-Design for optimal throughput. These tools are can leverage IC Validator within the design environment to quickly perform physical verification at each step in the process to quickly achieve sign-off quality within a few design iterations.
IC Compiler uses the foundry supplied manufacturing rules to build, where possible, a correct by construction decomposable layout. The double patterning solution is independent of mask decomposition and the place and route engines do not perform decomposition based on the coloring information. Double patterning constraints are specified in the technology file and IC Compiler considers layout conflicts in terms of double patterning cycles and spacing to ensure that the design is double patterning compliant. This is a way to avoid the issues identified above by the alternative split and stitch methodology.

DPT clean means the placer must ensure adjacent cells meet minimum space requirements if the boundaries are the same color or if available flip cells or select suitable alternatives if available in the library. Figure 11 shows an example of legalizing placement for DPT compliance.

![DPT Placement Legalization](image)

The router needs to provide a 2-colorable solution at the end of design while minimizing the impact on area and runtime. The key to this is not just applying the DPT spacing rules blindly which would ensure DPT correctness but also lead to area explosion. Zroute, the router within IC Compiler, utilizes multiple techniques to ensure DPT readiness and applies them intelligently. Two of the techniques the router utilizes is the selective use of spacing rules and knowing when to apply which rules and when to apply other techniques. The second technique here looks at the routed patterns and ensures that there are no odd-cycles or DPT violations created so every route can go on an alternate mask.

Using these features and IC Validator In-Design, signoff-quality DRC convergence can be achieved in less iterations. This is even more critical at 20nm, where DRC detection and correction works hand-in-hand with double patterning technology to enable automatic corner case signoff violation detection and correction in the IC Compiler environment.

**Reliability Analysis**

MOS Reliability Analysis (MOSRA) in HSPICE and CustomSim™ offers an accurate and efficient solution for analyzing the degradation of integrated circuit performance over time as a result of MOS device aging. The solution accurately models the HCI and BTI aging mechanisms and analyzes their impact on circuit performance using actual circuit operation and stimulus. MOSRA comes with a built in aging model that is silicon proven down to 20 nm. It also gives modeling teams the flexibility to integrate their in-house models. MOSRA is tightly integrated with the powerful engines in HSPICE and CustomSim, running post-stress analysis as fast as pre-stress runs.

**Custom Design**

As previously mentioned, 20-nm processing technology introduces new layers between the traditional front-end-of-line (FEOL) and back-end-of-line (BEOL) phases. These new layers are termed as middle-of-
line (MOL) layers or more colloquially as ‘local interconnect’. These all but disappeared at 40nm and 28nm but are being employed once again to provide very high-density local routing that helps significantly reduce extraneous intra-cell connections on the BEOL layers that could compromise pin access. Electrical connection between local interconnect layers and some of the FEOL layers is established by a simple overlap and unlike the traditional metal layers does not require a via. These layers are used only for short connections due to their electrical properties, but avoid the consumption of scarce routing resources on the lower DPT layers. Connectivity analysis and the interconnect creation commands have been augmented to include support for MOL in Galaxy Custom Designer layout editor.

The complexity of process rules for 20nm has increased significantly. There is a strong need for assistance to the layout engineer to produce design rule correct layout. Galaxy Custom Designer offers design rule driven (DRD) layout capabilities to guide the user in this regard. For 20nm, these technologies have been augmented to include support for complex via rules and rules that include the MOL layers.

20nm also introduces a special form of double patterning for the poly layer; in the first step a regular “grating” pattern for the poly layer is created. In the second step, a trim mask called “cut poly” layer is used to remove sections of the poly layer to generate the desired shapes. Thus during layout creation, the connectivity of the shapes on the poly layer is influenced by the presence of shapes on the trim mask. Galaxy Custom Designer introduces new technology to manage and manipulate the connectivity information due to such structures.

**What Is Next?**

The traditional planar transistor used with all CMOS devices up until now is proving very difficult to manufacture at 20nm. The ability to control the gate and avoiding large leakage currents has been a major challenge to continue to scale devices beyond 20nm. Foundries have been exploring alternatives and are expected to introduce multi-gate devices also known as FinFETs or Tri-gate FETs. Synopsys has been working actively with leading foundries in the early stages of creating this technology using Technology Computer-Aided Design (TCAD) tools that use computer simulations to develop and optimize semiconductor processing and devices. An example of a FinFET is shown below in Figure 13.
This new type of device is showing significant promise in enabling the semiconductor industry to go beyond 20nm and to continue designing more complex, high-performance devices at lower power levels. These types of devices have already been used at an earlier node and may even be introduced at 20nm. Synopsys has been supplying a number of tools to bring this new technology to market and are committed to delivering a complete solution via the Galaxy Implementation Platform.

**Conclusions**

The 20-nm process node is proving to be a challenging node requiring many fundamental changes in the design flow. The manufacturing requirements can no longer be isolated to post implementation activities. To achieve signoff closure and manufacturable devices, each of the major steps in the design process need to follow foundry rules and consider them as a part of the power, performance and area optimizations. The variations anticipated with the use of double patterning may introduce timing variations that must be modeled and the design analyzed for in addition to other checks needed at previous nodes, adding a further complexity to the design process.

To accomplish these goals in a timely manner, a much tighter integration between all parts of the tool-chain will be required. This close interoperability between process design, device implementation and manufacturing tools will be instrumental in maximizing the potential of this technology.

This new node will enable the semiconductor industry to further the levels of integration, increase the performance and lower the power consumption that consumers are looking for. Synopsys has already upgraded the key tools within the Galaxy Implementation Platform to be double pattern compliant and is collaborating closely with the industry’s leading foundries and semiconductor suppliers to introduce the first production devices.

**References**

Links to Synopsys’ 20-nm articles, videos can be found on the 20-nm solution web page:

[www.synopsys.com/20nm](http://www.synopsys.com/20nm)