Physical Design Assistance

**Highlights**

- Complement your design team experts with leading-edge physical design expertise
- Adopt design best practices and new methodologies
- Dedicated project assistance from synthesis to tape-out

**Proven Flows and Implementation Experience to Optimize Your Block Or Chip**

With each new process node, getting your block or chip design optimized, signed off and into volume production becomes more and more difficult, especially as competitive pressures increase and market windows shrink. Leveraging the integration benefits offered by very deep submicron (VDSM) processes, requires detailed knowledge of the strong interdependencies between timing, signal integrity, power distribution, power consumption and testability that amplify the challenges in physical design. The risk and expense of a long implementation cycle to meet your performance, power and area goals can impact your time to market and cost.

Through hundreds of projects and more than 20 years working on our customers’ most challenging projects, Synopsys Professional Services has built up leading-edge expertise to help you achieve optimized block- or chip-level implementation of your physical design in the fastest timeframe possible. Our consultants use their extensive experience with Synopsys’ world-class tools, Galaxy™ Design Platform and RTL-to-GDSII flows, including the production-proven Lynx Design System.

We deliver project support from the earliest phase of design planning through tape-out, identifying and resolving bottlenecks, and transferring methodology and best practices throughout the engagement. From block-level optimization, hierarchical design implementation, low power design and optimization, full-chip implementation, IP integration and constraints management to design closure and chip finishing, Synopsys experts can help you meet your goals.
Physical Design Assistance

Synopsys’ services include assistance with:

- Hierarchical constraints budgeting and design planning
- Design closure and signoff for static timing, EM/IR and SI
- Library data, design RTL, IP block and design constraints qualification
- Clock tree performance and power optimization
- Block- and chip-level power planning and optimization
- Routing closure and post route optimization
- Parasitic extraction and In-Design physical verification
- Block and chip finishing to signoff and tape-out
- Support for RTL-to-GDSII or netlist-to-GDSII handoffs
- Exporting demonstrated methods and baseline scripts for follow-on project use

To get more information on how we can customize our services for you, please contact Synopsys Professional Services or call your local sales representative.