

Synopsys Professional Services

Verification Consulting with VMM Methodology

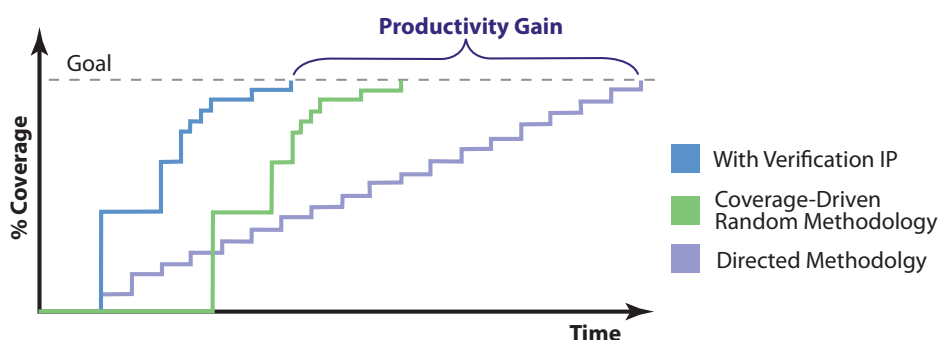
Apply the latest techniques to maximize your verification productivity

As traditional verification methods continue to fall behind in their ability to deal with increasing SoC complexity, advanced verification methods such as constrained-random stimulus generation and coverage-driven verification have emerged as effective methods for eliminating functional bugs and enabling first pass silicon success. Synopsys' Discovery™ Verification Platform is an integrated verification solution based on industry standards that encompasses the latest tools, IP and proven methodology to increase your verification productivity. Synopsys Professional Services can help you accelerate adoption of the industry's most advanced verification technologies and apply them to your design projects.

The *Verification Methodology Manual (VMM) for SystemVerilog*, co-authored by Synopsys and ARM, defines a coverage-driven, constrained-random methodology that speeds the time to reach coverage goals. The VMM methodology specifies guidelines for verification best practices that enable users to create a verification environment with more coverage in less time and with less code. The recommended testbench architecture is based on a layered approach for building a modular test environment that facilitates reuse. Synopsys delivers the industry's most complete VMM-compliant tool flow, and our consultants leverage their extensive expertise with the tools and experience in complex design to help you plan, architect, and deploy advanced verification flows.

At-A-Glance

- Methodology consulting to add advanced verification techniques to your flow
- Project assistance to help you build or migrate to a VMM-based verification environment
- A SystemVerilog Jumpstart is available to train new adopters



Synopsys consultants can help you deploy advanced verification methods and IP that results in significant gains in verification productivity.

Intellectual property (IP) cores have become a critical part of implementing complex SoCs. Pervasive use of third party IP poses challenges for both the implementation and especially for the verification teams. To address these challenges and further reduce the verification environment development time, Synopsys' DesignWare® IP portfolio includes a comprehensive set of production proven verification IP (VIP). The titles include several industry standard protocols such as AMBA 3 AXI, AMBA 2.0, PCI Express, USB 2.0 and OTG and Ethernet (10/100/1G/10G) etc. These VIPs seamlessly integrate with a VMM-compliant environment increasing ease of deployment. Synopsys consultants can assist you with integration of these VIPs so that you can quickly verify your design's compliance with the relevant standards.

Synopsys' comprehensive RTL verification solution, VCS®, supports popular design and verification language standards such as Verilog, VHDL, SystemVerilog, SystemC and Vera®, enabling faster validation of complex SoCs. Synopsys consultants also help users of Vera, testbench automation tool to build and extend the existing verification environment using VMM methodology.

Whether new to advanced verification methodologies and looking to accelerate your learning curve, or far along in your adoption and wanting to accelerate your testbench development, Synopsys consultants possess the tool and methodology expertise as well as the experience in verifying complex designs that will make your team more productive and your schedule more predictable.

Synopsys' verification consulting services include assistance in the following areas:

- Developing a robust test plan
- Architecting a VMM-compliant testbench that facilitates reuse across multiple sites and projects
- Creating infrastructure for generating constrained random stimulus
- Constructing bus functional models including both drivers and monitors
- Integrating verification IP/reference models
- Automated functional coverage collection to fine-tune random stimulus generator
- Building and integrating scoreboards to dynamically predict DUT response
- Deploying temporal checks using SVA/OVA checker library to facilitate debug

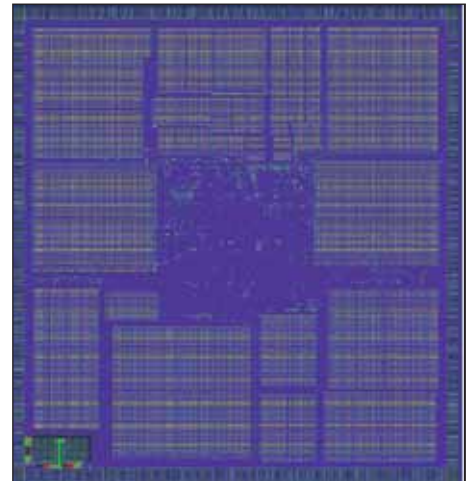
Case Study: Advanced Methods Ensure First Pass Silicon Success

Chongqing Chongyou Information Technology Co. (CYIT), a leading Chinese fabless semi-conductor company, develops chips for China's new 3G wireless communication standard, TD-SCDMA. Close cooperation and project management between Synopsys Professional Services and CYIT throughout the design process – from specification review through functional verification and chip implementation – ensured efficient project execution and tapeout success. The verification methods employed by Synopsys ensured high functional coverage for the multi-core chip and provided CYIT with an advanced, reusable methodology that improved the productivity of their verification environment. Producing

a fully functional chip with the first prototypes represented an important milestone for CYIT and helped it achieve its next round of funding.

“As we planned this project, we wanted to work with the best technology and the best design services partner. We selected Synopsys' Discovery Verification tools and Synopsys Professional Services and were rewarded with a successful chip tapeout and new methodologies that enhanced our design flow for our future designs.”

**– Professor Zhen Jianhong,
General Manager, CYIT**



For more information about Synopsys Professional Services, visit us on the web at www.synopsys.com/sps, contact your local sales representative, or call 866.537.6654.

Synopsys Professional Services: Helping to solve your toughest design challenges

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700 East Middlefield Road, Mountain View, CA 94043 T 650 962 5000 www.synopsys.com

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