

Synopsys and Tessera

Advanced verification flow enables rapid creation of high-quality IP



TESSERA® “Synopsys Professional Services consultants brought practical, important verification expertise to our design team.

They not only helped us meet the scheduled delivery of a critical design block, but they also developed and deployed a robust verification flow in the process.”

Hari Chakravarthula, Director Systems Engineering, Tessera

Tessera is a leading provider of miniaturization technologies for the electronics industry. The company provides a broad range of advanced packaging, interconnect and consumer optics solutions which are widely adopted in high-growth markets including consumer, computing, communications, medical and defense electronics. Tessera collaborated with Synopsys Professional Services to verify a complex graphics IP block and migrate it from an FPGA implementation to an ASIC. A key deliverable was the development of an advanced flow that ensured exhaustive verification of the IP block.

Synopsys Solution

- VCS®, LEDA®, Design Compiler®-Ultra, Formality®, TetraMax®, PrimeTime®
- Verification flow and test plan development
- Automation (scripts) for coverage-based verification runs and analyses
- RTL-to-Netlist implementation (Synthesis, DFT), Timing Closure

Cooperation Benefits

Synopsys design consultants helped Tessera define a verification strategy and then execute the test plan. Consultants also assisted with the modification and coding of several RTL blocks. The gate-level netlist was delivered with timing closed

and DFT-clean. To facilitate reuse and productivity in future projects, consultants provided detailed scripts, documentation and training for the functional verification, synthesis and formal verification flows. Most importantly, the joint teams were able to meet Tessera’s goal of a 33% reduction in gate count as part of an FPGA-to-ASIC conversion; this was achieved by using advanced features of DC-Ultra, such as register retiming.

