

Synopsys and ITRI

Establishing a New Production Flow for Low Power SoCs



**Industrial Technology
Research Institute**

“Our latest chip was developed with very challenging power optimization goals and targeting a new process node. Synopsys consultants worked closely with us to not only deliver the tapeout under a very tight schedule, but to also ensure advanced methodologies were built into our design flow. We are now recommending this flow to our 90 nanometer customers.”

– Dr. David Chang, Deputy General Director, SoC Technology Center/ITRI

The SoC Technology Center of the Industrial Technology Research Institute (STC/ITRI) is a leading industrial research lab devoted to developing innovative semiconductor technologies for Taiwanese companies and the global R&D community. In response to increasing demand from government and industry for advanced devices, ITRI engaged with Synopsys to establish a low-power design flow for 90nm and validate the flow through tapeout of its Parallel Architecture Core (PAC) DSP. The PAC DSP is a low-power, high-performance 32-bit programmable DSP core designed for next-generation media-rich and multifunction portable devices.

Since one of ITRI's objectives was to benchmark overall performance of the PAC DSP including frequency and power consumption, Synopsys and ITRI focused on the development and application of new methodologies and flows built around industry-leading tools from Synopsys' Galaxy Design Platform. Synopsys consultants, leveraging experience at 90nm and 65nm process nodes and the latest tool features, evaluated implementation trade-offs and optimization techniques with ITRI's designers.

Synopsys Solution

- Design Compiler® Ultra, PrimeTime® SI, PrimeRail
- Methodology Consulting to implement top-down power synthesis flow
- Physical design assistance through tapeout

Cooperation Benefits

Close collaboration between ITRI and Synopsys engineers resulted in the establishment of one of ITRI's recommended flows for 90nm with optimizations for power management. The team implemented advanced dynamic power techniques included clock gating, power-aware clock tree synthesis and placement, and multi-voltage automation, as well as multi-V_{th} and power gating to address leakage power. Power distribution integrity was achieved through power network synthesis (PNS) and full-chip power network analysis (PNA). The full combination of power management techniques in the flow and VDSM experience led to substantive savings in power consumption in the successfully implemented PAC DSP.

