

Implementation with Galaxy Design Platform

The Proven Approach to an Accelerated Tapeout

At-a-Glance

- ▶ *Complement your design team with experts in SI, power, DFT, DFM, and verification*
- ▶ *Qualify, optimize and assemble IP from multiple sources into a single chip implementation*
- ▶ *Adopt best-practices and new methodologies through knowledge transfer*
- ▶ *Design handoffs at specification, RTL or netlist stage with project support through tapeout*
- ▶ *Full concept-to-packaged parts capability*

Whether due to unexpected changes in project staffing or a strategic outsourcing decision, augmenting your design capability with Synopsys' design consultants can significantly improve your project productivity. In addition to design experience and tool expertise, Synopsys' design consultants leverage proven design flows and methodologies, program management best practices, and an extensive compute infrastructure to meet your program objectives. In short, our consultants bring the knowledge, technology and resources you've come to trust from Synopsys.

Specializing in RTL to GDSII design implementation at 130 nanometers (nm), 90nm, 65nm, and now 45nm, Synopsys Professional Services addresses the deep submicron challenges of timing closure, power optimization and management, signal integrity (SI), design-for-test (DFT), and design-for-manufacturability (DFM) to achieve predictable sign-off. Our expertise with Synopsys Galaxy Design™ and Discovery™ Verification platforms will help you maximize chip performance and avoid costly iterations.

Design teams can also utilize Synopsys' web-based design infrastructure; this collaborative "virtual" environment enables the project team to leverage people and compute resources anywhere in the world, any time of the day. Additionally, access to an extensive server farm with scalable hardware and software resources accelerates productivity during critical phases.

Rapid IP creation, qualification and integration are critical aspects of SoC development. Leveraging design reuse methodologies pioneered by Synopsys, we help you create high quality, reusable IP blocks. Our consultants also possess unique knowledge of Synopsys DesignWare® IP, the industry's most widely-used portfolio of IP cores and building block libraries. They will assist you in optimally configuring and integrating DesignWare's digital and mixed-signal IP. If your SoC includes a proprietary subsystem, we can create custom IP "wrappers" that interface industry-standard IP to your proprietary buses.

Synopsys' design services are flexible. Design activities can be fully collaborative, or you can handoff to Synopsys at virtually any level of abstraction (e.g., specification, RTL, or netlist). Our consultants are supported by a worldwide network of design centers and design experts that can be leveraged to scale with your project's changing needs. The significant experience of our consultants in designing some of the most advanced chips on the market enables us to be productive from the first day we're on the job—to get your SoC completed on time and on spec.

Application	Process geometry	Gate count	Clock frequency	Foundry	Services provided
Broadband	90nm	2.5M	250 MHz	TSMC	SoC integration, RTL handoff to GDSII
Wireless	65nm	1M	533 MHz	IDM	SoC integration, Multi-power flow
Computing	130nm	3.4M	400 MHz	TSMC	Integration and placed gates; handoff to GDSII
Wireless	90nm	13M	250 MHz	TSMC	RTL handoff to GDSII
Computing	90nm	23M	650 MHz	TI	RTL handoff to GDSII
Wireless	65nm	10M	235 MHz	TSMC	Physical design assistance
Networking	130nm	16M	250 MHz	TSMC	Block optimization and SoC integration
Consumer	65nm	50M	2 GHz	IDM	RTL handoff to GDSII
Wireless	90nm	10M	250 MHz	TSMC	RTL handoff to gates
Consumer	90nm	6M	533 MHz	TSMC	SoC integration, RTL handoff to GDSII
Graphics	90nm	5M	350 MHz	UMC	RTL handoff to GDSII

Typical Design Realization services include some or a combination of the following design tasks:

Block Optimization

- ▶ Micro-architecture and RTL code optimization
- ▶ Physical synthesis and block finishing to GDSII

Full Chip Integration

- ▶ IP qualification and configuration
- ▶ IP and block assembly and design capture for hierarchical designs
- ▶ Block and chip-level constraints management and integration

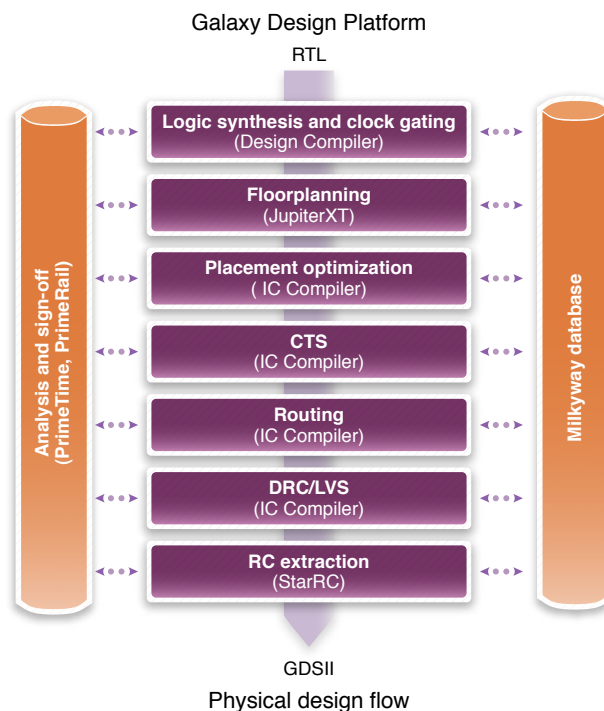
Physical Design Optimization

- ▶ Early library and IP qualification and generation of missing views
- ▶ Early floorplanning and power budgeting to address VDSM physical effects
- ▶ Interface logic modeling and static-timing analysis
- ▶ Signal integrity (SI) analysis and prevention
- ▶ Power analysis, dynamic and leakage power optimization
- ▶ Placement optimization with physical synthesis, clock-tree synthesis, and extraction
- ▶ SI-aware, OCV-aware, and yield-aware place and route
- ▶ Chip finishing and analysis
- ▶ Flat, hierarchical, and “virtual flat” flows for various chip complexities

Expertise in Physical Design

As process geometries shrink, the physical design process becomes an increasingly important factor in determining chip quality, yield and reliability. That’s because the physical effects at advanced process nodes of 130nm and below become first-order effects. When it comes to solving the complexities of physical design, there’s no substitute for experience. The most advanced tools in the hands of experienced engineers working with the best methodologies and infrastructure are the best ways to mitigate project risks.

Synopsys Professional Services has a long track record of successful chip tapeouts with and for our customers. Our design consultants utilize Synopsys’ leading-edge EDA technology and the Lynx Design System, a configurable, production-proven design flow with built-in utilities and methodologies for improving designer productivity. This IC development platform, configured for your specific design needs and proven on your chip, can be fully deployed during or after project completion to be leveraged on the next project.

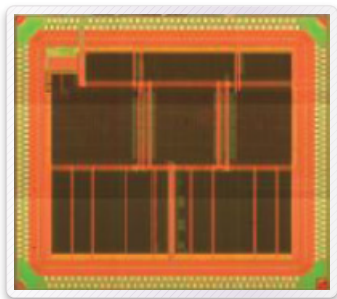


Case Study: Establishing a New Production Flow for Low Power SoCs

The SoC Technology Center of the Industrial Technology Research Institute (STC/ITRI) is a leading industrial research lab devoted to developing innovative semiconductor technologies for Taiwanese companies and the global R&D community. In response to increasing demand from government and industry for advanced devices, ITRI

engaged with Synopsys to establish a low-power design flow for 90nm and validate the flow through the tapeout of its Parallel Architecture Core (PAC) DSP low-power core designed for next-generation media-rich and multifunction portable devices such as media players, PDAs, and smart phones. Synopsys and ITRI focused on the development and application of new methodologies and flows built around industry-leading tools from Synopsys' Galaxy

Design Platform. Our consultants, leveraging substantial experience with 90nm and 65nm process nodes and the latest tool features, evaluated implementation trade-offs and optimization techniques with ITRI's designers. The full combination of power management techniques in the flow and VDSM experience led to significant savings in power consumption and first-success silicon.



“Our latest chip was developed with very challenging power optimization goals and targeting a new process node. ...We are now recommending this flow to our 90 nanometer customers.”

Dr. David Chang
Deputy General Director, STC/ITRI

Case Study: First Time COT, First Time Right

M-Systems is a leading developer of innovative, high volume data storage solutions for consumer applications such as mobile phones, PDA's, set-top boxes, and embedded systems.

Deploying a complete, pre-validated RTL-to-GDSII design flow from Synopsys enabled M-Systems to mitigate the risk of taking over the physical design of their chips. By providing additional design assistance through tapeout, Synopsys Professional

Services facilitated a smooth chip implementation and first pass chip success. Synopsys' design flow provided the best optimization in area and power consumption, two critical issues for high volume chips serving the consumer market.

“Building in-house physical design capability for a COT manufacturing model was accomplished in just 3 months with the help of Synopsys Professional Services. Functional prototypes from first silicon put us well on the way to meet our important customer deliveries.”

Michael Mostovoy
Director of ASIC Department, M-Systems

Synopsys Professional Services: Helping to solve your toughest design challenges.
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