

SoC Design and Verification

At-A-Glance

- ▶ Translate requirements to detailed specifications and plans
- ▶ Rapid architecture exploration using proven system modeling & analysis
- ▶ Configure and integrate IP blocks and subsystems
- ▶ Apply the latest methodologies to maximize your verification productivity
- ▶ Deploy new technologies and methods that improve hand-off between frontend and back-end design teams

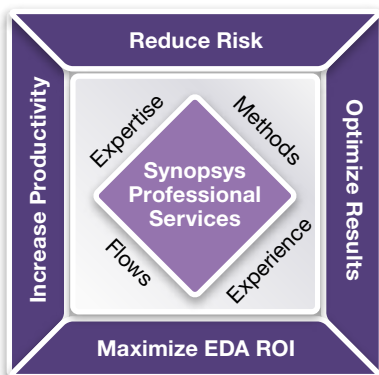
Achieve Rapid Design Closure By Applying Best Design Practices From The Start

The quality of early design deliverables such as the chip specification, RTL code and functional verification plan has tremendous impact on the efficiency of an SoC's implementation phase. In addition, the growing number and complexity of IP blocks and subsystems being integrated into today's SoC designs challenge even the most experienced design teams, particularly when the IP is new or otherwise unfamiliar to the team.

Synopsys consultants possess the expertise and experience to assist you in every stage of the SoC design, from the earliest phases of determining design feasibility and performance estimates through IP configuration and integration as well as verification and implementation. Synopsys designers can work directly with your system-level designers to ensure the design specifications accurately capture design intent at both the block and chip levels, helping to minimize iterations between the architecture and RTL implementation to increase productivity. We can then assist your team in translating the specification into a high-quality RTL description following best practices pioneered by Synopsys, as well as help identify and configure suitable IP blocks and subsystems to meet the design goals.

Rapid IP creation, qualification and integration are critical aspects of SoC development. Leveraging proven design reuse methodologies, we help you create high quality, reusable IP blocks. Our consultants also possess unique knowledge that will help you optimally configure and integrate Synopsys DesignWare® IP, the industry's most widely-used portfolio of IP cores and building block libraries. If your SoC includes a proprietary subsystem, we can create custom IP "wrappers" that interface industry-standard IP to your proprietary buses.

Verification remains the single most significant challenge in getting advanced SoC devices to market. The development of an independent verification plan, separate from the RTL creation, is key to generating an efficient functional verification approach which will minimize functional bugs. And because traditional verification methods simply cannot scale with chip complexity, our verification experts will help you take advantage of advanced verification techniques such as assertions, constrained-random stimulus generation, and coverage-driven verification, and rapidly deploy them across your entire project. Our consultants share expertise



with Synopsys' Discovery™ Verification Platform tools and apply best practices based on UVM as well as the proven methodology defined in the popular Verification Methodology Manual (VMM) for SystemVerilog, co-authored by Synopsys and ARM. Creating a design environment with VMM / UVM-compliant building blocks takes less time and eases cross-site collaboration as well as reuse at the block, system and project levels. By helping you employ the best design practices and the latest design methodologies in the front-end of the design cycle, Synopsys Professional Services enables you to achieve significant gains in overall design and verification productivity throughout the entire design process, and improve the predictability of your project schedule.

Synopsys' SoC Design and Verification consulting services include assistance with:

- ▶ Design Feasibility
 - Analyze power, performance, area, complexity, design effort, risks, etc.
 - Vendor-neutral assessment of technology options
- ▶ Specification and Plans
 - Capture and analysis of design requirements
 - Creation of detailed functional and verification specifications based on requirements
 - Definition of IP block configuration
 - Test strategies and plans
 - Prototyping plan
 - Timing for all operating and test modes
 - IP qualification metrics
 - Project metrics, tracking system
 - Resource and schedule estimates
 - Technical/schedule risk mitigation plans

- ▶ Architecture
 - Analyze CPU and DSP capabilities
 - Analyze Bus bandwidths and latencies
 - Analyze DMA performance
 - Define memory maps
 - Identify appropriate IP titles
 - Select optimum technology
 - Establish low power strategy
 - Partition for FPGA-based prototyping
- ▶ IP configuration and integration
 - Selection of IP titles and qualification
 - IP configuration
 - On-chip-bus architecture and topology design
 - Development of IP wrappers
- ▶ RTL coding and verification
 - Translation of functional specification into RTL description
 - Early use of design and coding guideline checker (LEDA) to detect potential RTL issues
 - Develop, verify reusable custom logic
 - Configure, integrate, verify IP blocks at IP subsystem and chip top levels
 - Create timing and power constraints
 - Construct and verify low-power circuits
 - Development of custom blocks
 - Incorporate early floorplan timing to reduce PD handoff iterations
 - Bind SystemVerilog assertions to RTL for verification coverage
- ▶ Developing a robust verification plan
 - Translation of verification specification into golden model and testbench
 - Architecting layered, automated testbenches
 - Code and integrate client, Synopsys and third-party VIP utilizing reusable testbenches, scoreboards, checkers, coverage bins

- ▶ Deploying advanced verification methodologies for
 - Constructing bus functional models with both drivers and monitors
 - Generating constrained random stimulus
 - Automating functional coverage collection to fine tune random stimulus
 - Deploying SystemVerilog assertions (SVA) or OpenVera assertions (OVA)
 - Optimize regressions to complete coverage plan efficiently
 - Check and verify low-power design
 - C/ASM software-driven verification
- ▶ FPGA based prototyping
 - Setup tool scripts, inputs and outputs, timing constraints
 - Map ASIC RTL, IP, clocks and memories to FPGA resources
 - Plan debug strategy vs. FPGA resource and timing constraints
 - Optimize wireload models vs. synthesis runtime for timing closure

SystemVerilog Jumpstart Training

In addition to project-based verification services, Synopsys consultants also provide dedicated Jumpstart training for customers who are new to SystemVerilog.

The SystemVerilog Language and Methodology Jumpstart for Verification from Synopsys helps chip developers understand and apply SystemVerilog's key features and benefits using Synopsys' comprehensive VCS® verification solution. Through five to seven days of intensive, classroomstyle instruction and hands-on labs, participants learn the skills required to create a reusable, productive and robust verification environment based on SystemVerilog's built-in support for constrained-random, coverage-driven and assertion-based verification.

Synopsys will customize the SystemVerilog Testbench, Assertions, and VMM / UVM Methodology training based on your needs and level of experience with SystemVerilog concepts. Detailed training agendas will be determined at the start of the Jumpstart engagement.

After completing an intensive series of courses customized to your skills and needs, you should be able to:

- ▶ Build a VMM / UVM-compliant verification environment in SystemVerilog
- ▶ Write an object-oriented re-usable testbench
- ▶ Generate constrained random stimulus to verify a device-under-test
- ▶ Create a predictor model to automate results checking
- ▶ Write assertions for dynamic simulation
- ▶ Apply functional coverage to measure completeness of tests

To get more information on how we can customize our services to help you meet your design goals, please contact us or call your local Synopsys sales representative.



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