

# HX5000 Design Flow and Infrastructure



**Honeywell and Synopsys Enable  
Next Generation Rad-Hard ASICs**

**Honeywell**

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**SYNOPSYS®**

## Overview

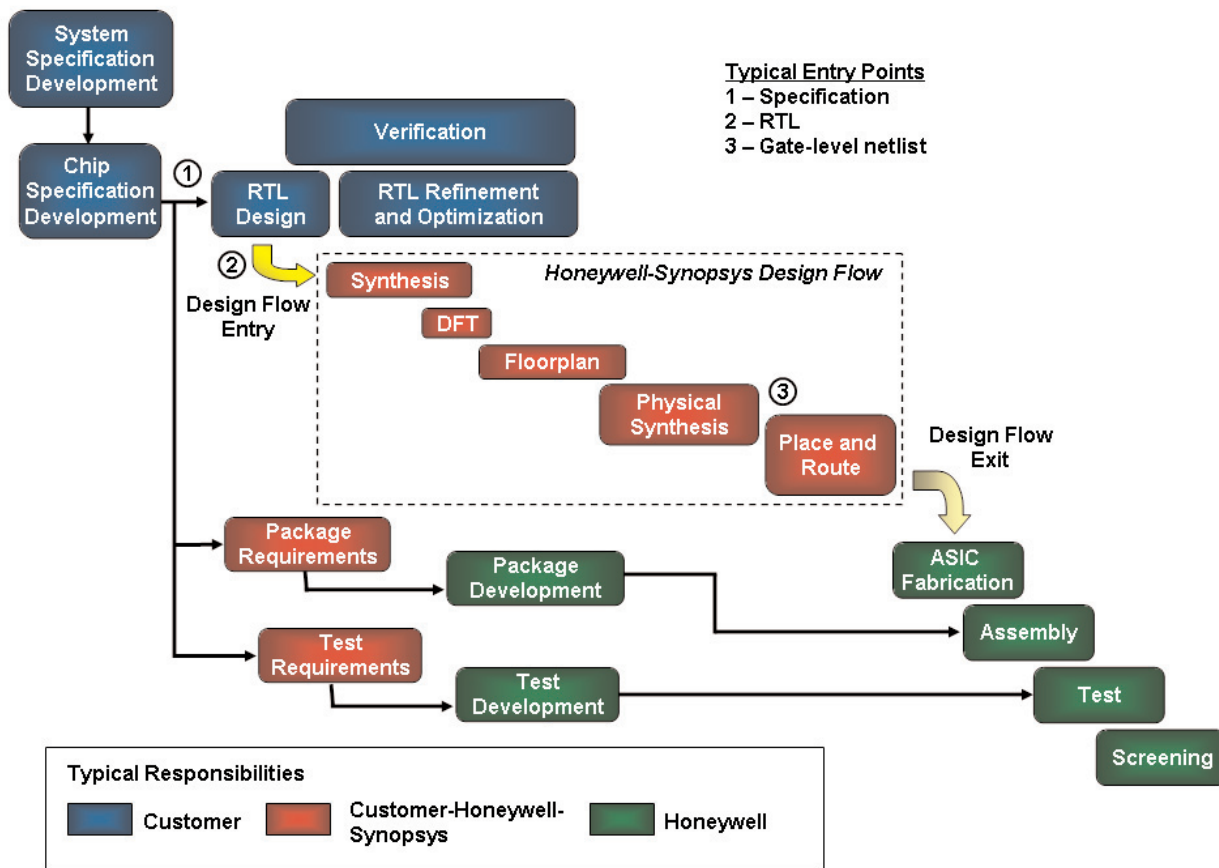
Radiation-hardened application specific integrated circuits (ASICs) can now achieve extremely high gate counts and speeds through the combination of a specially targeted silicon-on-insulator (SOI) semiconductor fabrication technology with a very deep submicron (VDSM) design flow. Through a portfolio of collaborative ASIC design and manufacturing services from Honeywell and Synopsys, military and aerospace (mil/aero) developers can achieve gate counts as high as 12-million gates

or more utilizing a 150-nanometer (nm) rad-hard manufacturing process. Honeywell and Synopsys have developed a unique collaborative design flow that enables efficient implementation of custom designs into HX5000 ASICs. The optimized design flow provides the industry's most comprehensive development capability for radiation-hardened (Rad-Hard) and radiation-tolerant (Rad-Tolerant) ASICs.

## Flexible design resourcing to address VDSM chip complexity

As ASIC designs expand in gate count and complexity, design teams require both increased capacity as well as a more diversified skill set to ensure the required expertise can be applied to specific design tasks. The collaborative design environment created by Honeywell and Synopsys provides a development model that is more flexible than traditional ASIC options. Along with support for traditional and expanded ASIC

handoff options, implementation support may include design services available from Honeywell and Synopsys Professional Services in a fully collaborative design model. This design support complements customers' existing design competencies and priorities, and can include the design of some or all of the ASIC as required to meet project schedule requirements.



**Figure 1** – The flexible, collaborative ASIC development process. Honeywell and Synopsys have teamed to provide comprehensive support at all stages of ASIC development. Though the most common customer handoff point is RTL, handoffs can also be at the specification, netlist or placed gates stages. Customers get back fully tested, packaged parts.

## Achieving commercial-level performance with rad-hard ASICs

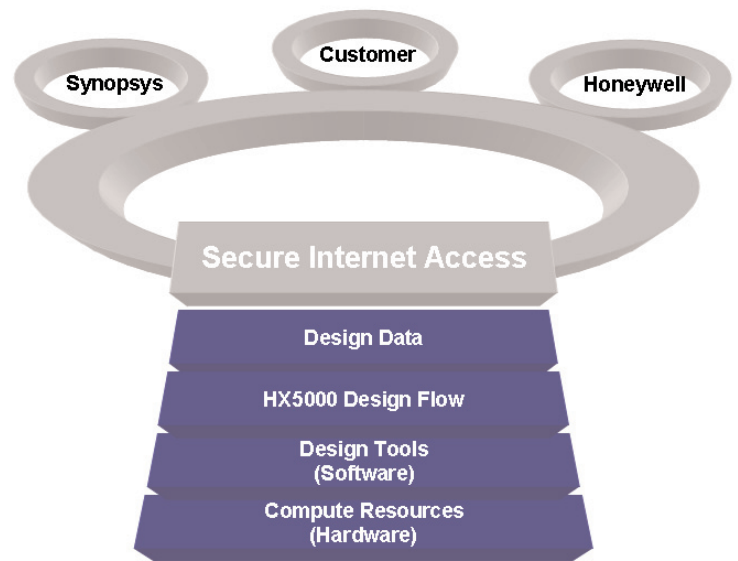
By using the Honeywell HX5000 ASIC design solution, designers can take advantage of a state-of-the-art rad-tolerant/rad-hard SOI process, an optimized design flow and highly productive design infrastructure jointly developed by Honeywell and Synopsys. This design environment includes access to:

- Honeywell's 150-nm SOI process technology
- Leading-edge Synopsys EDA tools and flow for designing and verifying complex ASICs
- A flexible set of front-end and back-end design services from design teams expert in the implementation of advanced ASICs and the HX5000 design flow
- A secure, web-based design environment with scalable compute resources that enables collaboration from multiple sites
- Access to intellectual property (IP) cores from Honeywell and Synopsys' DesignWare® IP, that accelerate design time and reduce development costs
- Qualified standard-cell libraries supporting both rad-hard and rad-tolerant design

## The efficiencies of cooperation: The design collaboration environment

With the level of device densities that are possible with 150-nm rad-hard ASICs, the infrastructure for effectively managing people, data, and hardware and software resources is critical to project success. Often design teams and resources are distributed amongst multiple sites, an outgrowth of the increased complexity and breadth of skills required for modern ASIC developments. During critical stages of the design, peak compute requirements often introduce bottlenecks.

To maximize design productivity, Honeywell and Synopsys have established the Design Collaboration Environment (DCE) illustrated in Figure 2. In addition to enabling real-time and secure sharing of design data, the DCE also provides on-demand access to design tools, along with extensive compute and storage capacity. The DCE enables engineers at multiple remote locations - including those of Honeywell, Synopsys and our mutual customers – to act together as a single design team with a unified design database and flow, applying the best expertise regardless of geography or time zone.

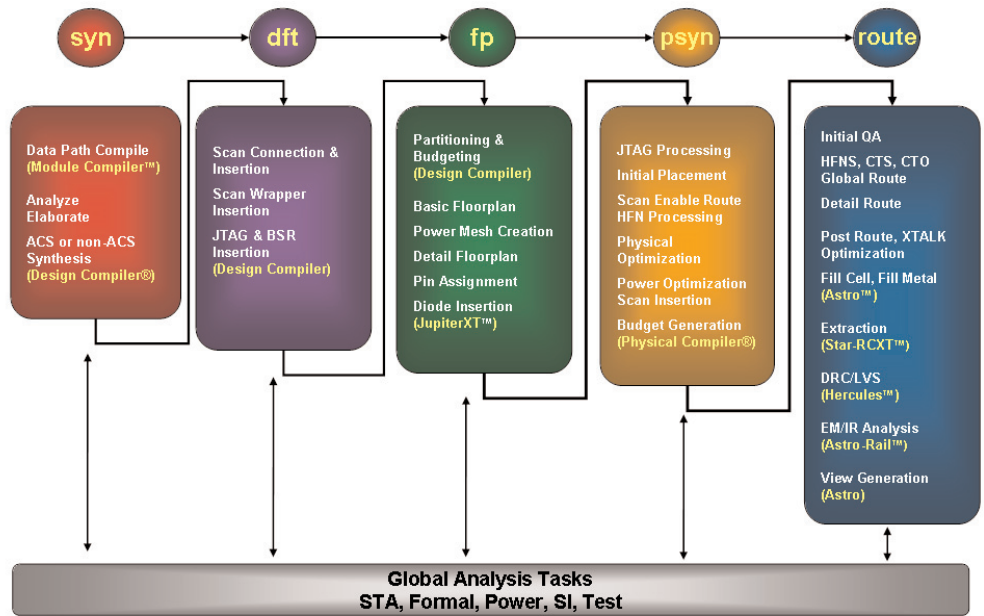


**Figure 2** – The Design Collaboration Environment provides a homogenous design environment and scalable compute resources. Secure Internet access makes it possible for remote resources to be applied for additional bandwidth or specific skill requirements.

The Honeywell-Synopsys design flow utilizes a validated sequence of tools and associated scripts from RTL through GDSII that allow designers to take maximum advantage of HX5000 capabilities (Figure 3a).

The Honeywell-Synopsys flow also includes procedures and tools to support radiation performance, including signal and cell EM (electromigration) analysis, and rad-hard power plan methods. The design flow supports built-in-test functions important for the reliability and electrical evaluation requirements of mil/aero applications such as:

- Memory BIST
- Scan and ATPG based testing

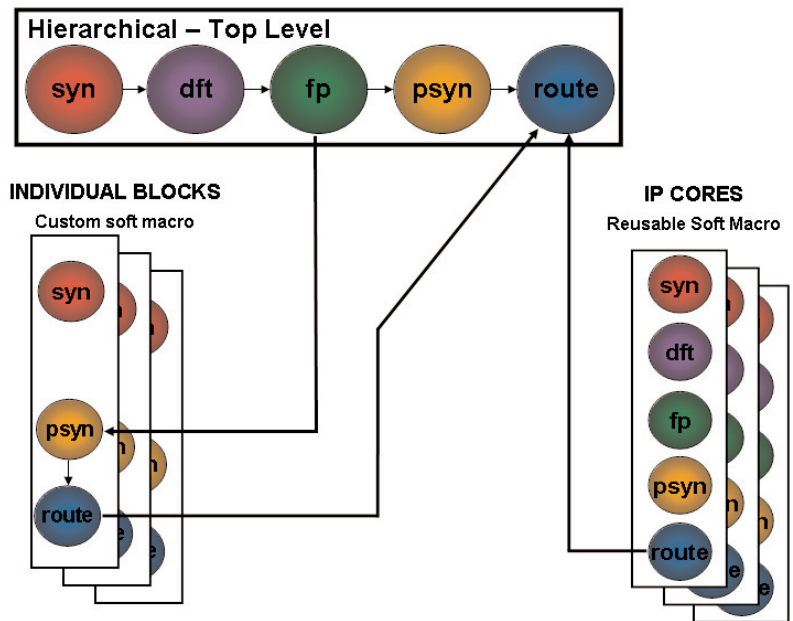


**Figure 3a** – The Honeywell-Synopsys design flow validated for 150-nm rad-hard ASICs takes designs from the RTL stage to final physical design.

### Silicon-proven ASIC design flow

The size and performance of designs coupled with the interdependencies of timing, power and signal integrity in VDSM design can lead to lengthy design iterations, making the design process highly unpredictable. The Honeywell-Synopsys design flow enables predictable design closure by incorporating:

- **Advanced tool flow** – concurrent optimization for timing, area, power, and signal integrity to meet all design goals.
- **Hierarchical design methodology** – for efficient management of multi-million gate designs by enabling a greater degree of design parallelism (see Figure 3b)
- **Consistent data model** – pre-defined directory structures, version control and job launching enable large teams to work effectively, even from multiple locations.
- **Flow control and automation** – *make-file* based flow automation and automated log-file parsing of errors decreases manual checks and enables fast flow reruns for design changes at the late stages of a project.



**Figure 3b** – The hierarchical design methodology with separate block, core and top-level flows keeps the design process predictable. Optimized sub-flows for synthesis (syn), design-for-test (dft), floorplanning (fp), physical synthesis (psyn) and routing (rt) are employed at each level of hierarchy as needed.

## Semiconductor intellectual property solutions

When designing ASICs with gate counts exceeding 10 million gates, custom design of all functional blocks is not practical. The use of silicon-proven design and verification IP (VIP) blocks for non-proprietary functions of the chip can provide a significant cost and time savings, and increase the probability of first pass success.

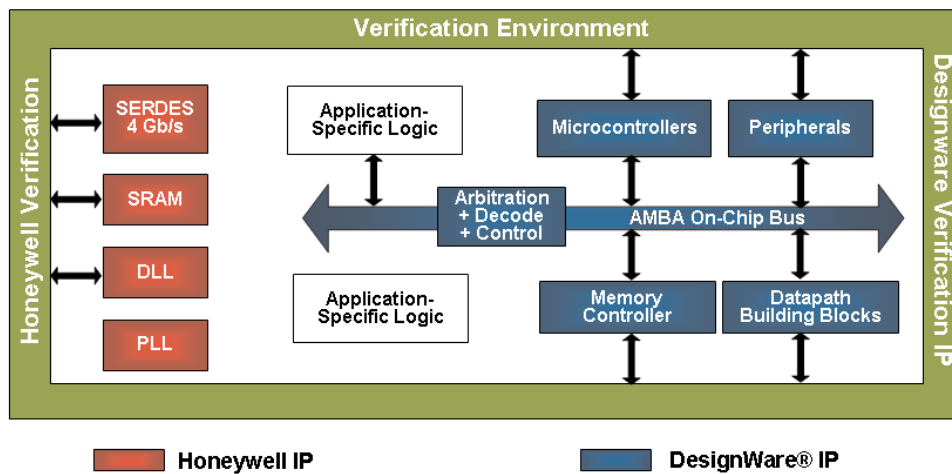
Along with a versatile Honeywell standard cell library, Honeywell silicon-proven IP is available for HX5000 ASICs. The Honeywell IP includes a serializer/deserializer (SerDes) core for backplane data communication at total data rates as high as 4.125 Gbps, and a family of synchronous and asynchronous embedded SRAMs optimized for rad-hard and rad-tolerant applications. To support high clock rates and I/O data rates, Honeywell macros also include mixed-signal functions such as Delay Lock Loops (DLL) and Phase-Locked Loops (PLLs).

In addition, HX5000 ASIC customers have access to Synopsys' DesignWare® IP portfolio. This IP has been validated in silicon

throughout the broader semiconductor industry on multiple foundry processes and is available as synthesizable, RTL soft macros. A broad range of IP blocks for datapath, I/O (e.g., USB, and PCI-X), AMBA™ on-chip bus functions and controllers are available.

Verifying the functionality of multi-million gate designs is a significant challenge that can consume the majority of the overall ASIC development effort. Verification testbenches can help designers reach verification goals faster and with improved functional coverage through quick and efficient creation of sophisticated testbenches. Synopsys' DesignWare IP portfolio includes the industry's broadest suite of verification IP with advanced features such as constrained random stimulus generation and coverage analysis.

Figure 4 shows a collection of IP typically found on advanced ASICs and available from Honeywell and Synopsys, including both functional and verification components.



**Figure 4** – Semiconductor intellectual property available for HX5000 rad-hard ASICs include SERDES, Embedded SRAMs, and interface blocks. Verification IP is also available as part of a testbench for improving verification productivity.

## A new era for mil/aero ASICs

The ability to build high performance radiation-hardened ASICs creates a new, higher level of capability for military and aerospace applications than ever before. Fully supported with an advanced design flow, a wide range of pre-verified IP cores, and a unique collaborative design environment, the HX5000 rad-hard ASIC design solution enables the development of sophisticated designs with a scale of integration previously unattainable for applications which require radiation hardened ASICs.

For more information about design solutions from Honeywell and Synopsys, please contact:

**Honeywell: 1-800-323-8295 or [www.myspaceparts.com](http://www.myspaceparts.com)**

**Synopsys: 1-866-537-6654 or [www.synopsys.com](http://www.synopsys.com)**

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