

HAPS Jumpstart

Specialized Training and Setup for Adopters of HAPS FPGA-Based Prototyping Solutions

At-a-Glance

- ▶ *On-site HAPS hardware and software flow training*
- ▶ *ASIC prototyping methodology development*
- ▶ *Working example of RTL to FPGA mapping based on your design style*
- ▶ *HAPS hardware setup and configuration*

Overview

Synopsys' HAPS[®] (High-performance ASIC Prototyping System™) solution is a modular and extendable system of hardware boards supported by an integrated tool flow that includes Synplify[®] FPGA synthesis, Certify[®] design partitioning, and Identify[®] interactive debugging software. HAPS is ideal for IP and SoC design and verification teams who take advantage of FPGA-based prototyping to find “corner case” hardware bugs or to start software development and integration in advance of ASIC availability.

The HAPS Jumpstart training helps designers understand and apply near real-time SoC prototyping methodology using Synopsys' HAPS. The Jumpstart training delivers five days of on-site services to assist you in setting up a comprehensive FPGA-based prototyping flow customized for your design environment. The collaborative, hands-on deployment model accelerates the integration of prototyping into your overall verification plan while advancing your design team's knowledge of FPGA-based prototyping methodologies and implementation.

Synopsys will adapt the HAPS Jumpstart to your team's experience level with FPGA-based prototyping. Typical Jumpstart engagements include:

Prototyping Flow Training

Classroom-style instruction provides new HAPS users with hands-on training that covers key tool features and methodologies using a sample design. The duration and topics for the training vary based on users' expertise and project requirements. A typical multi-day agenda covers the following:

- ▶ RTL design for FPGA implementation
- ▶ Logic synthesis for FPGA
- ▶ Partitioning large designs into multiple FPGAs
- ▶ Detailed analysis of hardware results to facilitate debug
- ▶ Xilinx place-and-route software overview

Planning and Setup

Once users are familiar with the HAPS flow, a review of your verification plan and prototyping goals is conducted. This review enables Synopsys consultants to assist you in creating a prototyping project plan that specifies the appropriate setup and configuration required. Portions of your actual RTL code can be used to setup

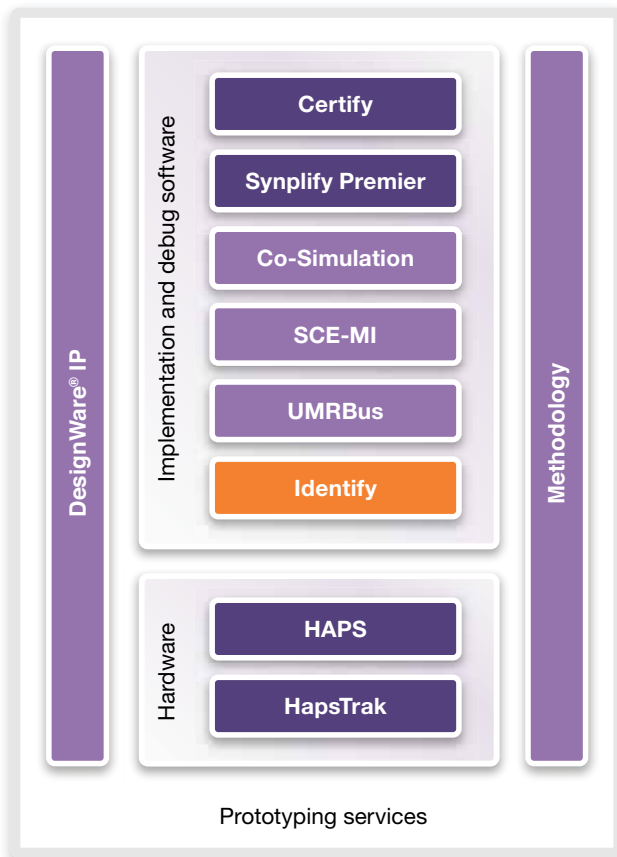


Figure 1: Integrated FPGA-based prototyping flow

and illustrate the key aspects of the prototyping flow, including:

- ▶ Handling gated clocks
- ▶ Mapping ASIC memories to FPGAs
- ▶ Partitioning and pin-multiplexing to map large designs
- ▶ Strategies and options to facilitate design debug
- ▶ 3rd-party IP considerations for FPGA implementation
- ▶ Evaluating optimal prototyping performance vs. effort
- ▶ Analyzing Design Compiler® scripts to determine constraints
- ▶ Configuring hardware clocking resources

Upon the completion of this phase,

examples of the ASIC-targeted design mapped for FPGA and HAPS hardware should be in place.

HAPS Hardware Configuration

Once the flow is set up and the RTL design is ready for FPGA mapping, HAPS is configured. Using the HAPS hardware available at your site, your engineers will get hands-on experience configuring HAPS to address:

- ▶ Specific power supply connections and built-in self-test
- ▶ Component connectivity and clock configuration setup
- ▶ Supervisor control circuit configuration
- ▶ JTAG interface setup between the workstation and HAPS

- ▶ Hardware remote control configuration via LAN
- ▶ Debug and visibility instrumentation using MICTOR cards, a logic analyzer and Synopsys' Identify® RTL debugger

Additional Training (Optional)

Depending on participants' familiarity with FPGA-based prototyping, Synopsys consultants can augment the Jumpstart training in the following areas:

- ▶ Certify® Pin Multiplexing (CPM) or the automated High-speed Time-Domain Multiplexing (HSTDM) feature to time-share I/O pins
- ▶ Synplify® Premier features for in-system debug and faster timing closure
- ▶ Utilize fast data transfer with UMRBus technology
- ▶ In-depth HAPS hardware configuration
- ▶ HAPS custom daughter card considerations

Jumpstart Prerequisites

- ▶ Certify software license installed
- ▶ Xilinx ISE software license installed
- ▶ Xilinx JTAG download cable available

The following are recommended in order to ensure the most efficient Jumpstart training delivery schedule:

- ▶ Required HAPS components available on-site
- ▶ Certify-compiled RTL code
- ▶ Lab area for system setup and HAPS hardware

For more information about Synopsys products, support services or training, visit us on the web at:

www.synopsys.com, contact your local sales representative or call 650.584.5000.

Synopsys Professional Services: Helping to solve your toughest design challenges