

Accelerating Tool and Methodology Adoption

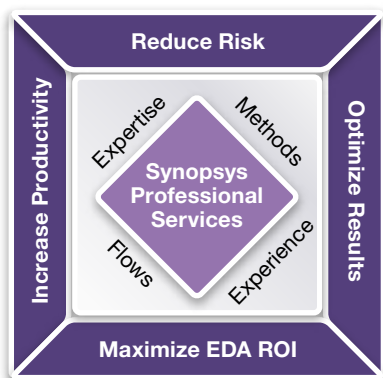
At-A-Glance

- ▶ Apply the latest tool features and methodologies to address specific design challenges like power and signal integrity
- ▶ Advance your design methods and practices through project-based assistance
- ▶ Accelerate your learning curve with new Synopsys technology

Take Full Advantage Of The Latest Tool Features And Methodologies

As a Synopsys customer, you realize how important it is to maintain a leading-edge design environment. Deploying the latest releases of Synopsys' tools and platforms provides tremendous gains in design productivity and quality of results through improved performance and new features. But the complexity of designs and implementation challenges at new technology nodes often allows little time to optimize your design environment with the most advanced EDA tool features and methodologies.

Synopsys Professional Services is experienced in Synopsys' technology-leading tools and platforms. Benefiting from our close ties to the tool developers and a broad resume of customer project experience, our design consultants are uniquely qualified to help you rapidly deploy the latest EDA technology into your flow. Synopsys design consultants continually receive extensive training to keep improving their design skills and tool knowledge. As you deploy Synopsys technology, Synopsys Professional Services will accelerate your learning curve and help you take advantage of new product functionality to improve your design productivity and accelerate your tapeouts.



Synopsys' Tool and Methodology Adoption services include assistance with:

- ▶ Migrating and customizing design scripts for new tool versions
- ▶ Methodology consulting to deploy design methods and best practices
- ▶ Applying new tool features through project-based design assistance
 - Design Compiler® Ultra: Library-aware mapping and structuring, data path optimization, critical path re-synthesis and topographical technology for accurate correlation to post-layout timing, area and power
 - Design Compiler Graphical: Virtual global routing technology to predict wire routing congestion during RTL synthesis
 - IC Compiler: Concurrent multi-mode, multi-corner optimization, advanced clock tree synthesis and post-route optimization, physically-aware scan-chain optimization, signal integrity (SI) and Multi-Vth leakage power optimization, multi-voltage power optimization, MTCMOS leakage optimization, yield optimization
 - IC Compiler Zroute Technology: Advanced routing algorithms, concurrent DFM optimizations and multithreading
 - IC Validator: In-Design physical verification
 - PrimeTime® Suite: HSPICE-accurate analysis, CCS modeling, automated hold fixing, ILM/ETM-based hierarchical static timing analysis, on-chip variation (OCV), signal integrity signoff, comprehensive power analysis extension, vector-free analysis, variation aware statistical timing
 - VCS®: SystemVerilog for design and verification, coverage analysis

To get more information on how we can customize our services to help you meet your design goals, please [contact us](#) or call your local [Synopsys sales representative](#).



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