Job Description

Synopsys is seeking a creative, ambitious and talented engineer to fill a senior verification role in Japan, Tokyo. The environment presents stimulating, challenging and rewarding work within an excellent work environment with positive career development opportunities.

The successful candidates will work on product development for DDR memory controller or similar protocols. As these designs are part of the DesignWare portfolio it presents the opportunity for the successful candidate to have their work used in many of the leading products that are developed by Synopsys customers. The verification is challenging as the IP components themselves are complex and are used in a wide variety of applications. As a senior member of the team you will take a lead role in guiding other team members in the use of best practice verification techniques.

We develop best in class designs using the latest best practice in verification to ensure their quality and we need the right people to keep making this happen. As a worldwide organization there is occasionally short term travel required.

The ideal candidate will have

- A relevant degree in electronic engineering or computer science
- Knowledge of IC design flows
- A successful track record in relevant project work
- Good problem solving skills
- Good English communication skills
- Capability to produce adequate technical documentation
- Good working knowledge of Verilog or VHDL
- Good working knowledge of System Verilog or VMM or OVM or UVM
- Exposure to Unix, Perl and TCL scripting
- Willingness to learn new things
- Capability to work as a team member and promote excellent working relationships
- Knowledge of DDR memory controller or similar protocols would be advantageous

If you are interested in this position, please contact to jp-hr-saiyo@synopsys.com