Executive Summary

- Move to multicore designs leads to drop in clock speeds (pg 10)
- New chip gate dielectric promises big boost to equipment manufacturers (pg 7)
- CPU semiconductor IP declines, but IP categories confuse issue (pg 2)
- Interest in pure analog IP outpaces mixed-signal cousin (pg 9).

Complexity Increases While IP Categories Cloud Usage Trends
By Erach Desai

Analysis and Trends
Stop the presses! After several months of declining trends in overall system-on-a-chip (SoC) design activity and complexity, there may actually be some light at the end of the proverbial tunnel. There will be more information on such findings when we dive into...

...Continued on page 2

Behind the Numbers
By Dave Bursky

Why is Analog Integration Lagging Digital?
As companies continue the process migration to ever-smaller design rules, designers of analog circuits are facing additional challenges. Issues arise when they must co-integrate the analog functions on the digital chips. The smaller feature sizes will allow circuits to operate...

...Continued on page 6

45-NM CHIPS ARE ARRIVING SOONER THAN EXPECTED
Even as most companies struggle to get their first 65-nm circuit designs completed, designers at Intel Corp. and IBM Corp. have demonstrated that 45-nm-based designs are possible. In the second half of this year...

...Continued on page 7

Analog IP -- Ready for Prime Time?
By Geoffrey James

IP Trends
The Gordian knot of electronic design automation (EDA) is making analog designs as easy to automate as digital designs. Every few years or so, a handful of companies emerge with promises that analog EDA is right around the corner. Yet those promises always fall by the wayside when the problems outstrip the technology. Today, the prevailing theory is that...

...Continued on page 9

Predictions: Clock Speeds Level Off in Q107 Due to Multicore
By John Blyler

Performance, Power and Area
The art – and even the science – of making predictions are fraught with peril. Many factors must therefore be considered in developing accurate prediction models. Even then, nothing is...

...Continued on page 10
the nitty-gritty of the data analysis for this month’s issue. The current issue of Chip Design Trends reflects data that has been accumulated through the month of December 2006. Aside from the fact that we are now tracking data on upwards of 38,500 unique design investigations, the number of design experiments for the month of December bounced back very nicely – and predictably - off the multi-month low-point achieved in November.

As always, one should be mindful that we collect and analyze data on SoC design investigations (or experiments), but not actual design starts per se. Yet the net analysis of this rich data set nonetheless reflects how new, complex, application-specific-integrated-circuit (ASIC) design starts are trending.

We’re continuing with the prior two issues’ multi-faceted analysis of design-complexity trends on a monthly basis. In this issue, we also have continued to drill down on the usage of processor intellectual-property (IP) cores with a focus on CPU cores.

As has been our custom, Figure 1 summarizes the data and analysis for SoC design investigation activity by geography. With the December 2006 data, we “naturally” end up with quarterly data for relevant comparison. Some key observations based on Figure 1 follow:

- Compared to the dynamics we observed for the three months ending November 2006, the rate of decline in total SoC design investigations improved somewhat in the fourth quarter of 2006. That is the silver lining. Design investigations declined by 44% in the fourth quarter of 2006 compared to the same quarter of 2005, which – at first glance - appears as a somewhat baffling overall trend. Furthermore, the sequential decline in overall design activity in the fourth quarter versus the third quarter of 2006 was 21%. This number clearly exceeded the more “seasonal” decline of 4% sequentially in the fourth quarter of 2005.
- As we’ve observed in the past couple of months, trends in North America largely mirrored the overall trends. The actual percentage declines were worse than the overall numbers. We would focus on the 30% sequential decline in design experiments in the fourth quarter of 2006, which was much worse than the flat sequential change in activity in the fourth quarter of 2005.
- With the fourth-quarter-of-2006 data, both Europe and Asia have started to demonstrate the same directional trends as North America: sequential and year-over-year declines (although the declines are more muted).
- Design activity in the rest-of-world (ROW) regions, as collected in our data-set, was just under 8% of overall design investigation activity for the fourth quarter of 2006. Nonetheless, these collective regions continue to show signs of significant growth (up 136% on a year-over-year basis and up 151% on a sequential basis).

While the raw monthly data for December 2006 improved from the nadir touched in November, we note the decline in overall design activity in the fourth quarter of 2006—especially when compared both to the third quarter of 2006 (more than “seasonal”) and the fourth quarter of 2005. Is this decrease in chip design investigations the result of the factors that Dave Bursky illuminated in the December 2006 issue of Trends (“Are ASIC Design Starts Tapering Off”)? Or will this month’s trends data shed addition light on the decrease in design investigations? Let’s see.

There are two important and constructive observations to be gleaned from Figure 2. First of all, the number of design investigations for each die-size range tracked

<table>
<thead>
<tr>
<th>Quarter Ending=&gt;</th>
<th>Sep ’05</th>
<th>Dec ’05</th>
<th>Sep ’06</th>
<th>Dec ’06</th>
</tr>
</thead>
<tbody>
<tr>
<td>N. America – Design Investigations</td>
<td>4,414</td>
<td>4,417</td>
<td>2,586</td>
<td>1,809</td>
</tr>
<tr>
<td>Year-over-year change</td>
<td>-41%</td>
<td>-59%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sequential change</td>
<td>+0%</td>
<td>+20%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Europe – Design Investigations</td>
<td>1,318</td>
<td>1,018</td>
<td>910</td>
<td>840</td>
</tr>
<tr>
<td>Year-over-year change</td>
<td>-31%</td>
<td>-17%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sequential change</td>
<td>-23%</td>
<td>-2%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Asia – Design Investigations</td>
<td>571</td>
<td>687</td>
<td>759</td>
<td>549</td>
</tr>
<tr>
<td>Year-over-year change</td>
<td>+33%</td>
<td>-20%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sequential change</td>
<td>+20%</td>
<td>-43%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ROW – Design Investigations</td>
<td>193</td>
<td>114</td>
<td>107</td>
<td>269</td>
</tr>
<tr>
<td>Year-over-year change</td>
<td>-45%</td>
<td>+136%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sequential change</td>
<td>-41%</td>
<td>+5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total – Design Investigations</td>
<td>6,496</td>
<td>6,236</td>
<td>4,362</td>
<td>3,467</td>
</tr>
<tr>
<td>Year-over-year change</td>
<td>-33%</td>
<td>-44%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sequential change</td>
<td>-4%</td>
<td>-4%</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 1: Clearly, there is a continued downtrend in new design activity.
upwards compared to what happened in November. In addition, our average die-size trend line has moved higher for two consecutive months (and nearly at 40 mm²). These trends would support a thesis of moving toward more complex designs.

Consistent with what we’ve noted in prior months, the die-size “sweet spot” continues to remain below 50 mm². Curiously, but not surprisingly, the 50-to-75-mm² range appears to also be breaking out--although the logarithmic scale can be deceptive.

In Figure 3, we capture the monthly trends in SoC design experiments by process technology node layered with a weighted average of process node. The average process node is very definitely trending lower for four consecutive months. (Lower is good in this case!) It is approaching 110 nm, which would also make intuitive sense. Consistent with recent monthly data, the raw numbers also confirm that the bulk of design investigations are clustered around 90, 130, and 180 nm.

Over the past couple of months, the 250-nm process node showed a marked and sustained drop (in terms of number of design investigations targeted to that process geometry). On an intuitive basis, this trend would reaffirm a broader thesis of gradually moving to more complex design activity.

Figure 4 captures the frequency of design investigations by the targeted number of metal interconnect layers deployed for leading-edge SoC designs. Ignoring the somewhat schizophrenic average trend line, we instead focus our attention on the six-month trailing average. The lumpiness of the November data wasn’t helpful to the trend line. Yet it’s fair to observe that we are hovering in the 6.3 to 6.4 layers-of-interconnect range.

In past issues (December 2006), we’ve noted that many new designs are run through foundry shuttle programs (or targeted to be run through such programs for design investigations). This is likely the most obvious explanation for 6LM being the workhorse of new design activity. Thus, we wouldn’t expect any “breakout” beyond the 6 to 7 LM range until the foundry shuttle programs migrate toward a higher level of interconnect “standard.” Nonetheless, Figure 4 continues to add to a mosaic of data supporting the move to more complex SoC design activity.

After five successive months of declining, the average for the highest targeted clock speed (for SoC designs being tracked) has moved up nicely in the past two months. December jumped to nearly 350 MHz. The trailing-four-month, moving-average trend line now appears to be consolidating around 200 MHz, as depicted in Figure 5.

Higher clock speeds have historically been correlated (or associated) with more complex SoC designs. In this era of consumer-oriented devices, however, higher clock speeds imply more power consumption and
thus a deleterious impact on battery life. On balance, we would suggest that a trend line of modestly higher clock speeds continues to support a thesis of more complex SoC designs, as long as the highest clock speeds don’t spike too much.

Still, another factor that would account for the lower clock speed trend is the migration of newer designs to a dual ported memory architecture that runs at a lower “bus rate” but achieves a higher throughput. Externally, the net effective clock rate is actually going up, thanks to the higher serial data rate of the SerDes interfaces which utilize the common PHYS protocols (up to the 5+GHz range). However, while the external throughput may be greater, the net internal word rate for these protocols has dropped to lower speeds.

Figure 6 graphs the monthly trends by I/O signal ranges with the now familiar “average” metric. The average pin count for our data set of complex SoC designs picked up nicely in December 2006. It appears to be hovering around 300 pins. Much like the metric of highest clock speed, trying to interpolate total pin count into a measure of SoC design complexity isn’t that simple. Historically, more complex SoCs have been associated with higher pin counts. Because there’s such application-specificity associated with pin counts and design function, it would be unfair to make that generalization. Furthermore, higher levels of integration (at smaller process geometries) might suggest that a good deal of “bus” bandwidth can be handled on chip rather than off chip. The need for linear growth in pin counts would therefore be alleviated.

A FIRST LOOK AT CPU SEMICONDUCTOR IP

Previously, we stated the obvious: Embedded memory and CPU cores are the most prevalent form of semiconductor IP (semi IP) deployed in complex SoC designs. In this issue of Chip Design Trends, based on our
proprietary database of design investigation trials, we thought it might be more incisive to focus on CPU IP cores. Before diving into that, however, let’s continue to track some of the initial trends that we started to analyze in the prior issue.

Figure 7 captures the use of multiple semi-IP cores (non-memory) on a monthly basis. At a fundamental level, one would expect the trend-line for multiple semi-IP cores to be steadily increasing over time, given macro trends (more complex designs) and intuition (more compelling usage of semi IP over in-house development). Again, our data doesn’t seem to bear this out. The average number of non-memory IP cores has been declining from about five per design a few months ago to roughly two per design.

Figure 8 dives into a second layer of detail: the use of unique CPU core instances on a monthly basis layered with our weighted average trend line. The first thing that jumps out from Figure 8 is the slow-but-steady move toward one unique CPU-core instance per design in recent months. For the second but equally pertinent observation, look at the average of north of three unique CPU cores per design nearly a year ago. There are two ways to interpret this data. We most likely don’t know which explanation holds true:

1. CPU cores become more complex per generation and thus do not need to be replicated in multiple instances.
2. There is a fundamental decline in the usage of multiple CPU instantiations per design (contrary to what complex SoC design trends would suggest).

Figure 9 depicts the distribution of non-memory semi-IP core usage across the dimension of soft macro usage versus hardened IP cores. As we noted last month, the graph clearly shows that the category of greater-than-80%-hard predominates in our database. Note that our data does not distinguish the relative complexity of semi-IP cores utilized for a particular design experiment. Thus, more “mundane” soft IP cores like USB and PCI-Express would get as much relevance in our analysis as that from a process-specific hardened CPU core from ARM, for example.

We know from Geoffrey James’s analysis in the last issue (“Co-Processor IP Market Prepares for Rapid Growth”), that interest in digital-core IP – a category that includes core-processor IP – is high. Further, recent industry data from companies like Samsung, Chartered, eASIC, Raza Micro, AMD Embedded, Intel Embedded, ARM, MIPS, IBM, Broadcom, and Qualcomm confirms that the semiconductor industry is moving toward multicore platforms that use both soft and hard IP. However, in reference to our above noted decline in CPU semi-IP, it must be noted that many of these major companies categorize their IP as “bit-slice”, not multicore. Semantics, semantics!

In future issues of Chip Design Trends, we hope to explore additional metrics for the usage of semiconductor-IP cores. At the same time, we will dig deeper into the inter-relationships between some of these metrics on a per-design investigation basis.
**CONCLUSION: COMPLEXITY RISING, BUT ACTIVITY MODERATING**

After several months of challenging data and disturbing trend-lines, we were glad to observe a nice bounce-back in overall activity for the month of December 2006. Furthermore, the complexity of new-design activity started to rise after several months of seemingly successive declines. (Complexity was measured by die size, technology process node, number of interconnect layers, and clock speed and pin count [both to a lesser degree]).

Before we pop open the champagne, however, it’s important to note that total SoC design experiments in the fourth quarter of 2006 declined by 44% compared to the fourth quarter of 2005 (year over year). Compared with the third quarter of 2006, those design experiments declined by 21% (sequentially). As we noted at the outset, the sequential decline cannot be simply explained away as “seasonality.” But it can be explained, at least in part, by the increasing complexity of designs which has lead to a decrease in overall design projects.

Finally, CPU semi-IP usage – in design investigations – seems to be declining, though this may be due to the inconsistent categorization of IP usage by the EDA-semiconductor industry as a whole.

As part of the full Chip Design Trends “package,” we plan to publish bi-annual reports that dive deeper into the numbers and technology trends of relevance. One goal for the numbers analysis section will be to look at overall semiconductor-market revenue trends, complex SoC design-start data (from market analysts), EDA-market revenue trends, and semi-IP-market revenue trends. We also will attempt to determine if there are connections and correlations between these various sets of data, including our own proprietary database of complex SoC design activity.

Erach Desai, Chief Analyst, Chip Design Trends

**Figure 9: Hardened semi-IP cores continue to dominate.**

**Behind the Numbers**

...Continued from page 1

at higher frequencies, thereby permitting chips to incorporate radios for Wi-Fi and WiMAX applications that operate at 2.4-GHz and higher frequencies. When moving analog functions to smaller design rules, however, many design challenges must be dealt with in order to meet the market demands in the analog market segment.

Analog technology represents a $33-billion market. About 60% of that market is dedicated to specific applications, according to Steve Ohr, Analog Research Director at Gartner Group, a market-research company. He explains that the design of such circuits requires a team effort comprising both digital designers and a smaller number of analog engineers, who implement analog functions in the digital domain and in CMOS.

To meet the performance demands in the analog market, many design challenges are related to the implementation of analog functions along with digital in advanced CMOS processes. These challenges arise due to higher leakage currents, trickier circuit layouts, and lower operating voltages. As transistors get smaller, minor variations in performance become important—even though they weren’t an issue at 130-nm and larger feature sizes. Because margins are reduced as the operating voltage goes down, device-to-device variations within a chip cannot be tolerated. To ensure that analog functions can deliver optimum performance, the following are needed: better process-monitoring tools to make sure that process parameters stay stable; improved layout tools to better match transistor sizes; and mirror shapes to create matched pairs and deal with even minor thermal issues during layout.

As features scale down, however, the lower operating voltage may be the most
critical issue of all. Most of today’s 90-nm designs operate at supply voltages of 1.5 to 1.8 V. At 65 nm, though, most circuits are expected to operate with 1.2-V supply levels. That may continue to drop to 1 V or less as design rules drop to 45 nm and below. Such lower operating voltage may limit the dynamic range that the analog circuit can handle. This limitation, in turn, could compromise some of the signal-processing operations that the circuit may have to perform.

For example, a smaller dynamic input range for an analog-to-digital converter (ADC) limits the signal swing that the converter can handle. It forces the converter to use smaller voltage increments to deliver 10-bit resolution for, say, a 1-V signal swing. A resolution of 10 bits roughly translates into a 1-mV increment for each change from 0 to 1 V. Yet a 12-bit converter would reduce the increments to just 250 mV. Still higher-resolution converters will demand even smaller, stable increments. The smaller the step, the harder it is to achieve stability over a range of temperatures, power-supply variations, and various internal-component drift factors.

To achieve the stable and repeatable operation of ADC and other analog functions, designers are actually leveraging digital technologies to add various self-correction modes and auto-calibration capabilities into the converter or other analog function. Although this approach adds some overhead into the analog function, it can greatly improve overall circuit performance. The self-tuning can null out error sources so that converters can deliver full resolution and accuracy, offsets can be eliminated, and other performance-detracting variations can be hidden.

As design rules shrink, analog designers will increasingly depend on digital technology to help compensate for the issues that arise due to smaller features. This trend will allow analog designers to continue to leverage the latest design rules without sacrificing circuit performance. Of course, the design rules for analog circuits may still lag by one or two generations versus digital design rules. But this lag won’t equate to the three- or four-generation difference seen in recent years.

Dave Bursky, Contributing Editor, Chip Design Trends

Figure 1: The conventional polysilicon-gate/silicon-dioxide-gate structure used for transistors over the last 35 years or so (left) will be replaced by Intel with a metal gate and hafnium-based high-k dielectric (right). This dielectric promises to deliver lower leakage, faster switching speeds, and lower-power operation.

45-nm chips are arriving sooner than expected

...Continued from page 1

Intel has even promised to start commercial manufacturing of the first five in a series of 15 45-nm-based dual-core processors (410 million transistors). The change in process technologies that is required to implement circuits using 45-nm design rules promises to affect more than just the lithography supply chain. This change goes beyond shrinking the features and controlling the dopants.

In Intel’s recent announcement, for instance, it detailed the company’s use of a Hafnium-based oxide to achieve high k values for the dielectric layer between the gate electrode and the silicon (see Figure 1). What was not as obvious about the announcement was that the oxide will be deposited one molecular layer at a time via atomic-layer deposition (ALD). Although this oxide-deposition technique has been in limited
use by a few memory-chip manufacturers, it hasn't been used for logic chips.

The use of ALD will require new fab equipment in any fab that wants to implement ALD material deposition. Chemical/material suppliers also will have to produce the Hafnium sources needed by the ALD equipment. As a result, there will be new opportunities in the supply chain. The higher k value possible with Hafnium will allow designers to deposit a thicker oxide layer between the gate and the silicon—approximately 10 atomic layers. Gate leakage will therefore be reduced by more than tenfold, improving circuit performance.

In contrast, today’s 65-nm processes typically use a gate-oxide layer about five atomic layers thick. Such a thin layer allows larger gate leakage currents. If that layer were to scale below five atomic layers, leakage currents would escalate and transistor performance would degrade. The thicker layer thus eases manufacturing constraints. In addition, it could improve overall circuit yield (see the cross section in Figure 2).

But Intel didn’t stop there. The company made another major improvement by employing metal-gate electrodes rather than polysilicon for the gate electrode. This change to the gate material reduces the gate resistance. It also allows for sharper and deeper turn-on/turn-off characteristics for the individual transistors. The deeper turn-off reduces drain-source leakage current. In doing so, it lowers overall leakage power by more than fivefold. The sharper turn-on/turn-off characteristics improve transistor switching speeds. These benefits, coupled with the reduced parasitic losses of the 45-nm features, reduce overall transistor switching power by about 30%. They also allow for a doubling of the transistor density, which could lead to smaller chips at a set density level or much more complex chips in the same chip area.

According to company Co-founder, Gordon Moore, “The move to the new gate dielectric and metal gate structure by Intel is the biggest change in transistor technology since the introduction of the polysilicon gate MOS transistor in the late 1960s.” Mark Bohr, an Intel Senior Fellow responsible for logic technology development, agreed that this represents a significant change in materials. Yet Bohr notes that it also allows Intel to retain its use of 193-nm optical lithography. As a result, it doesn’t have to transition to the more expensive immersion lithography systems. Furthermore, all previous process enhancements, such as the use of strained silicon to improve transistor performance and the use of copper metallization for low-resistance interconnects, can be retained.

As important as the new material is to improving transistor performance, the method for introducing it into current manufacturing techniques to maintain compatibility with the process flow can be equally important, notes Dr. T.C. Chen, Vice President of

![Figure 1: Using extreme magnification, the actual atomic layers of silicon can be seen at the bottom of this photo of Intel’s 45-nm transistor structure. Above the silicon, the thin, dark, solid region is the high-k hafnium-based oxide. Above that is the metal gate, which has a low-resistance capping layer over it.](image)
the only way to automate analog design is to use analog intellectual property (IP) to speed circuit design.

As any EE who’s worth his or her silicon will tell you, analog circuitry can be mind-bendingly complex, forcing designers to wrestle with dozens of variables and parameters. What’s worse, analog components need more power and cause more electrical interference than digital ones. Fortunately, some analog circuitry is beginning to become standardized. In some cases, it is therefore making it possible to reuse the same analog IP inside different chip designs.

“Analog IP can result in significant savings in design costs because, in most cases, the only other approach is to design from scratch,” observes John Koeter, Group Director of IP and Services Marketing for Synopsys, which is heavily deployed in the IP sector. He further notes that integrating analog into system-on-a-chip (SoC) designs becomes even more challenging as designs move below 90 nm. “As chip components get smaller, there’s less voltage available for power-hungry analog and a greater likelihood of problems,” he explains. “The solution, obviously, is to reuse analog IP as much as possible.”

In fact, Koeter cites analog IP as a primary engine behind an estimated $1.4 billion worldwide yearly market for IP. “Analog and mixed-signal IP is our fastest growing segment,” he says. Indeed, Design Trend’s own “IP Interest” analysis indicates gradually growing interest in analog IP—particularly the “pure” analog IP that’s the most challenging for chip designers (See Sidebar).

Koeter points out that the consolidation of the foundry industry (driven largely by the ballooning cost of fab-building) makes analog IP even more valuable. “With companies like Chartered, IBM, and Samsung pooling their resources, there are fewer unique manufacturing processes to support,” he says. “As a result, we’re ‘silicon ready’ with a number of designs that can be ported from fab to fab.”

Analog IP is still far from plug and play, though, warns Mahendra Jain from QualCore Logic, a maker of analog IP. “The problem is that every chip designer needs to use analog IP differently,” he states. As a result, most real-world uses of analog IP involve a significant amount of customization services—the very work that companies wish they could automate, according to Jordan Selburn, Principal Analyst with the market-research firm, iSuppli. Selburn notes, “A number of EDA companies have tried to automate the integration process but without general success to date.”

Yet “in the last few years, ‘some’ analog IP has matured to the point that you can buy it and use it,” says Gary Smith, erstwhile EDA Analyst for Gartner and an independent EDA consultant. Still, Smith counsels that any design effort involving analog IP is well advised to have at least some analog engineers on board. “Analog IP, even more so than digital IP, isn’t a replacement for engineering talent,” he notes. “It’s a productivity enhancer that gives your analog engineers time to work on the custom analog portion of the chip.”

In other words, analog IP—despite its usefulness—is a long way from cutting through the knotty problem of automating analog design.

Every month, we assess trends in the chip-design community based upon designer
usage of a leading IP portal. Data from the last three months indicates a growing interest in pure analog IP as opposed to varieties of mixed-signal IP. This trend probably reflects the greater ease of integration into multiple manufacturing processes. It is being reflected in sales of pure IP from major IP vendors like Synopsys, according to Norm Kelly, the company’s Director of Business Development for IP.

Geoffrey James, Contributing Editor, Chip Design Trends

Sidebar: IP Interest Map

Still, making well-reasoned predictions is an integral part of the business and technology worlds. Reliable predictions are based on past data trends and a keen understanding of the area being predicted. In our case, that “area” is the making of systems-on-a-chip (SoCs). With the ending of 2006, we now have enough historic data – over 38,500 unique design investigations extending over a two-year timeframe – and industry expertise to begin making predictions about future growth areas in the chip design industry. These predictions will be limited to a three-month window, which extends from our most current data set (e.g., from December 2006 to March 2007) for this issue (see Chart). Before examining the predictions for this issue, let’s “do the numbers.”

Total design investigations for December 2006 experienced a sharp 77% increase from the previous month. They increased

Sources:
- John Koeter, Synopsys. Contact: Yvette Huygen, Yvette.Huygen@synopsys.com
- Norm Kelly, Synopsys. Contact: Yvette Huygen, Yvette.Huygen@synopsys.com
- Mahendra Jain, QualCore Logic. Contact: Nanette V. Collins, nanette@nvc.com
- Jordan Selburn, iSuppli Corp., JSelburn@isuppli.com
- Gary Smith, GarySmithEDA.com, gary@garysmithEDA.com

Performance, Power and Area

...Continued from page 1
from 812 to 1439 investigations. Although it is reassuring, this increase in SoC investigations doesn't offset the overall decline from the fourth quarter of 2006 versus the same quarter of 2005 (see Erach Desai's section for more details).

Specific investigations into performance, power, and area parameters followed the general increase in total design numbers (see Figure). One point of interest is that design investigations at the most popular average clock speed, which is less than 100 MHz, increased at the slowest rate of the last two quarters. As our experts point out in this issue, this clock-speed stabilization is attributed to the growing interest in multicore designs.

According to our aggregated data, the most popular average clock speed in December 2006 remains below 100 MHz. Erach notes, however, that the highest clock speed is hovering around 200 MHz. In terms of die size, designers experimenting with future chip projects still favor chip areas of less than 50 mm square. This trend seems to support the continuing interest in smaller-process-node designs.

What does the future hold for the key technology indicators of performance (average clock speed, power, and area)? Our prediction is that February and March of this year will experience an increase in design investigations using chip power of less than 0.11 W, die size of less than 50 mm square, and average clock speed of less than 100 MHz. Perhaps the most significant part of this prediction is that clock speeds are leveling off, due in large measure to the growing interest in multicore – mainly multiprocessor – designs.

John Blyler, Editorial Director

Chip Design Trends is the only monthly newsletter and bi-annual report to capture the details of ASIC and ASSP chip design trends in the pre-silicon, exploratory performance-power-area tradeoff phase of SoC development.

Most existing chip design forecasts focus on the back-end, post-design stage of chip development - for example, semiconductor sales, equipment investment and foundry capital utilization. Unlike these back-end reports, Chip Design Trends draws from an estimated 25,000 project feasibility studies per year to provide detailed trends on the front-end, pre-silicon phase of SoC development. To learn more, visit: http://www.chipdesignmag.com/trends/
Chip Design Trends
Data, Analysis, and Benchmarking on SOC Design
www.chipdesignmag.com/trends

Copyright © 2006 by Extension Media LLC. All rights reserved. Reproduction in any form whatsoever is forbidden without express permission of copyright owner.

EDiTOrIAl StAFF
Editor-in-Chief
John Blyler (503) 614-1082
jblyler@extensionmedia.com

Erach Desai, Chief Analyst
erach@desaisive.com

Dave Bursky, Contributing Editor
dbursky@extensionmedia.com

Geoffrey James, Contributing Editor
gjames@extensionmedia.com

Clive “Max” Maxfield, iDesign Editor
cmaxfield@extensionmedia.com

Editorial Board
Tom Anderson, Consultant • Cheryl Ajluni, Technical Consultant, Custom Media Solutions • Karen Bartleson, Standards Program Manager, Synopsys • Chuck Byers, Director Communications, TSMC • Pallab Chatterjee, Consultant, Silicon Map • Rich Faris, Marketing Director, Real Intent • Kathryn Krane, CEO, Jasper Design Automation • Barry Marsh, Vice President Marketing, Actel • Tom Moxon, Consultant, Moxon Design • Walter Ng, Senior Director, Design Services, Chartered Semiconductor • Scott Sandler, CEO, Novas Software • Steve Schulz, President, SI2 • Adam Traidman, CEO, Chip Estimate

PRODUCtiON StAFF
Director of Production
Barney Lee (415) 255-0390 x13
blee@extensionmedia.com

Print Production Specialist
Ryan Teuscher • rteuscher@extensionmedia.com

SUBSCRIPTS ANd CuStOMEr SERvICE
To start your subscription, please visit the website at: http://www.chipdesignmag.com/trends or call: 1-866-834-1248.
Published 12 times per year on a monthly basis.

Rates:
• Chip Design Trends Newsletter: $695 per year
• Chip Design Trends Newsletter and two special bi-annual reports: $1,950

© 2007 Extension Media. All rights reserved.

(cont’d)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Designs Tracked by Ck Speed</td>
<td>1,248</td>
<td>1,254</td>
<td>1,927</td>
<td>1,162</td>
<td>1,574</td>
<td>1,901</td>
<td>2,113</td>
<td>1,496</td>
<td>951</td>
<td>1,571</td>
<td>812</td>
<td>1,439</td>
</tr>
<tr>
<td>≤100 MHz</td>
<td>689</td>
<td>767</td>
<td>1,011</td>
<td>739</td>
<td>755</td>
<td>1,232</td>
<td>1,382</td>
<td>911</td>
<td>743</td>
<td>1,215</td>
<td>565</td>
<td>612</td>
</tr>
<tr>
<td>&gt;100 MHz</td>
<td>559</td>
<td>487</td>
<td>916</td>
<td>423</td>
<td>819</td>
<td>669</td>
<td>731</td>
<td>585</td>
<td>208</td>
<td>356</td>
<td>247</td>
<td>827</td>
</tr>
<tr>
<td>≤ 100 MHz (Equivalent)</td>
<td>689</td>
<td>767</td>
<td>1,011</td>
<td>739</td>
<td>755</td>
<td>1,232</td>
<td>1,382</td>
<td>911</td>
<td>743</td>
<td>1,215</td>
<td>565</td>
<td>612</td>
</tr>
</tbody>
</table>

By Die Size

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>≤ 50 mm sq.</td>
<td>749</td>
<td>761</td>
<td>1,277</td>
<td>1,156</td>
<td>1,574</td>
<td>1,901</td>
<td>2,112</td>
<td>1,496</td>
<td>950</td>
<td>1,570</td>
<td>812</td>
<td>1,436</td>
</tr>
<tr>
<td>&gt; 50 mm sq.</td>
<td>585</td>
<td>673</td>
<td>1,059</td>
<td>886</td>
<td>839</td>
<td>1,431</td>
<td>1,668</td>
<td>1,194</td>
<td>771</td>
<td>1,357</td>
<td>676</td>
<td>1,080</td>
</tr>
<tr>
<td>≤ 50 mm sq. (Equivalent)</td>
<td>974</td>
<td>1,108</td>
<td>1,598</td>
<td>890</td>
<td>839</td>
<td>1,431</td>
<td>1,668</td>
<td>1,194</td>
<td>771</td>
<td>1,357</td>
<td>676</td>
<td>1,082</td>
</tr>
</tbody>
</table>