**Forward-Looking Statements**

This presentation contains forward-looking statements under the safe harbor provisions of Section 21E of the Securities Exchange Act of 1934, including statements regarding projected financial results and long-term growth rates. For a discussion of important factors that could cause actual results to differ materially from those in such statements, see the section entitled “Risk Factors” in Synopsys’ most recent Quarterly Report on Form 10-Q and Annual Report on Form 10-K.

**Regulation G**

In addition to financial results prepared in accordance with Generally Accepted Accounting Principles, or GAAP, this presentation will also contain certain non-GAAP financial measures. Except for certain forward-looking non-GAAP financial measures for which a reconciliation is not possible without unreasonable efforts, reconciliations of the non-GAAP financial measures contained in this presentation or given orally to their most comparable GAAP measures are included in the fourth quarter fiscal 2014 earnings release and financial supplement, dated December 3, 2014, and available on Synopsys' website at www.synopsys.com/Company/InvestorRelations/Pages/FinancialNews.aspx.
Synopsys Introduction

- **Global leader in Electronic Design Automation** (EDA), the tools and technologies used to design chips

- **Leading provider of semiconductor Intellectual Property** (IP), the reusable building blocks that are used for chip designs

- **The market & technology leader:** Virtually all leading-edge semiconductor designs in the world use Synopsys technology
## Synopsys Snapshot

<table>
<thead>
<tr>
<th></th>
<th>FY14</th>
<th>FY15 (Target*)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Revenue:</strong></td>
<td>$2.057B</td>
<td>$2.185 – $2.225B</td>
</tr>
<tr>
<td><strong>NG EPS:</strong></td>
<td>$2.53</td>
<td>$2.67 – $2.72</td>
</tr>
<tr>
<td><strong>Business Model:</strong></td>
<td>~90% time-based</td>
<td></td>
</tr>
<tr>
<td><strong>Revenue Sources:</strong></td>
<td>~½ International</td>
<td></td>
</tr>
<tr>
<td><strong>Employees:</strong></td>
<td>~9,440</td>
<td></td>
</tr>
<tr>
<td><strong>Market Cap:</strong></td>
<td>~$6.7B</td>
<td></td>
</tr>
<tr>
<td><strong>Founded:</strong></td>
<td>1986</td>
<td></td>
</tr>
<tr>
<td><strong>Patents Granted:</strong></td>
<td>~2,299</td>
<td></td>
</tr>
</tbody>
</table>

* These targets were provided by Synopsys as of December 3, 2014, and are not being updated at this time.
Synopsys: The Market & Technology Leader

Uniquely Positioned for Stability and Growth

- Dynamic markets
- Clear technology leadership
- Financial strength and growth
Global Value Chain

EDA & IP – At the Heart of Accelerating Electronics Innovation

- EDA & IP* $9.0B
- Embedded Software* $2.8B**
- Foundry $41.2B
- Semiconductors $348B
- Electronic Systems $1,488B

*Estimates are provided for EDA/IP/Embedded Software
** 2013 value
Source: IC Insights, VDC Research, Synopsys Estimates
Helping Design the Chips Inside
Impacting Everyone, Everything, Everywhere, Every Day

Mobile  Computing & Peripherals
Medical  Data Center & Networking
Automotive  Military / Aerospace
Cloud Infrastructure  Digital Home
Internet of Things  Industrial
Mobile

Global Internet Device Sales

Source: Business Insider's “2013 - The Year Ahead In Mobile”, January report

© Synopsys 2014
By 2017, the annual global IP traffic will surpass the zettabyte threshold (1.4 zettabytes).

Source: Cisco Systems, VNI Global Mobile Data Traffic Forecast Update 2013
Internet of Things

- Power
- Buildings
- Cars
- Toasters
- Lamps...

“Smart”
- Software
- Sensors
- Microprocessors
- Storage
- Communication

<table>
<thead>
<tr>
<th>Year</th>
<th>Lines of Code</th>
<th>SW &amp; E/E % Vehicle Cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970</td>
<td>100K</td>
<td>&lt;9%</td>
</tr>
<tr>
<td>1990</td>
<td>1M</td>
<td>33%</td>
</tr>
<tr>
<td>2010</td>
<td>100M</td>
<td>&gt;40%</td>
</tr>
</tbody>
</table>

Example: Buildings, Cars, Toasters, Lamps...?
Significant Growth in Sensors

Sensor Units to Grow to 30 Billion Units in 2017

Source: Semico Research, 2013
Semiconductor Design Complexity

- An advanced design today will take 18-24 months to complete, and can cost up to $200M.

- Design starts (total) have declined slightly over the past several years, but the complexity of those designs has increased exponentially, requiring more, and more advanced, EDA tools.

- As IC design complexity grows, there is the need to embed an increasing amount of IP.

- The adoption of FinFET technologies drives further design challenges.
Complexity Drives Demand for Tools

Synopsys Consistently Leads in Advanced Designs

Leading companies migrating to very advanced nodes; some waiting at 32/28nm

Many choosing to skip 22/20nm and go to 16/14nm FinFET

Ramp of 16/14nm FinFET appears robust

Our tools are used for all processes

Source: Synopsys Global Technical Services
Designs Are Becoming More Costly

**Primary Designs**

Note: Primary Designs are new and more-complex design(s), typically shipping in high-volumes, are developed on the next process node, require qualification on a whole new range of IP, and typically contain extensive software content.
First to 16/14nm Design

Synopsys Solutions Used in Every FinFET Design

- Samsung and Synopsys Collaborate to Achieve First 14-nanometer FinFET Tapeout (Dec, 2012)
- GLOBALFOUNDRIES and Synopsys Partner To Provide Comprehensive Design Environment for Foundry’s 14nm-XM FinFET offering (December 20, 2012)
- Synopsys and UMC Collaborate to Accelerate Development of UMC’s 14-nm FinFET Process (June, 2013)
- TSMC Certifies Synopsys Digital and Custom Solution for V1.0 N16 FinFET Process (April, 2014)

• Tracking >170 FinFET designs and tapeouts worldwide. Synopsys is integral to >95% of them.

Source: Synopsys Global Technical Services
Comprehensive FinFET Solution

Synopsys’ FinFET Leadership

- Have invested in the extremely fast-growing FinFET segment for almost a decade
- Comprehensive solution, ranging from TCAD to design tools, to IP, to sophisticated support
- Collaboration with key foundries
- Believe we have at least a year head-start over any competitor

“Clearly, from a technical point of view, Moore’s Law is alive and well, and Synopsys is central in driving it forward,” Aart de Geus, Synopsys Chairman and Co-CEO
Blue Chip Customer Base

- Customer base consists of virtually all semiconductor companies in the world, including all of the top 20
- One ~10% customer (Q414 & FY14)
- For many years we have collaborated closely with market leaders, including top foundries, IDMs and fabless customers
Synopsys: The Market & Technology Leader

*Uniquely Positioned for Stability and Growth*

- Dynamic markets
- Clear technology leadership
- Financial strength and growth
Broaderest Portfolio of Best-in-Class Technology

System Design

Verification
IP
Implementation

Manufacturing

Systems
SoC
Silicon
#1 in Core EDA

- 62% of current revenue; 4% trailing twelve-month revenue growth*
- ~90% of 20nm and below tape-outs have used Synopsys implementation
- Vast majority of advanced designs utilize Synopsys digital verification
- 19 of the top 20 semiconductor companies rely on Synopsys analog circuit simulation

Key Technologies

- Synthesis
- Place & Route
- Signoff
- Physical Verification

- Custom Design
- Digital & AMS verification
- Emulation
- FPGA Design

* As of December 2014
Introducing IC Compiler II
Game-Changer in Place & Route

Rebuild
New Infrastructure
- New Infrastructure
- Multi Hier
- Multi Mode
- Multi Thread
- Multi Voltage
- Multi View

Rethink
New Engines
- Timer
- Floor Plan
- Opt.
- Clock Tree

Reuse
Best of IC Compiler I
- Linear Placer
- Zroute

Enabling 10X Throughput
Early Customer Successes

A

10X Faster Placement Opt.
4X Faster Clock Opt.

Tapeout Underway

B

25M Instances in Under 4 hrs
10X TAT in Design Planning

Tapeout Underway

C

8X Faster Placement Opt.
2X Faster Clock Opt.

Tapeout Underway

D

6X Faster Placement Opt.
3X Smaller Memory

Tapeout Underway
Introducing Verification Continuum

- Game-changing new platform launched in 2014
- Seamless integration
- Built around best-in-class engines; adding unified debug, compile
- Goal: speed software bring-up by ~6 mos
- First deliverable: Verification Compiler 2014
- Additional integration in 2015
2014: Verification Compiler
Comprehensive, Best-in-Class Verification in One Product
Enable “3X” Verification Productivity
Introducing ZeBu Server-3

Industry’s Fastest Emulation System

Performance
Speeds HW/SW bring-up and SoC verification up to 4X for faster time-to-market

Hybrid Emulation
Links to virtual prototype for architecture optimization and early SW development

ZeBu Server-3: 300M gates in a 20” cube
< 2.5 kW, <155 pounds

Debug
Comprehensive debug with full signal visibility and Verdi³ integration

Architecture
Advanced architecture for lower total cost of ownership

Capacity
Industry’s highest capacity – scalable to three billion gates
#1 in Manufacturing

- 9% of current revenue; -2.5% trailing twelve-month revenue growth*
- Mask data prep tools used by 8 of the top 10 semiconductor manufacturers
- TCAD tools used by 9 of the top 10 semiconductor manufacturers
- Yield management solution reducing time to production yield

Key Technologies

- Mask Synthesis
- Mask Data Prep
- Yield Management
- TCAD

* As of December 2014
Growth in Core EDA + Manufacturing

Estimated Long-Term Organic Growth Rate

- Generally in the low-to-mid single digit range*
- Growth drivers:
  - Segment growth + market share gains

Segment Growth Drivers

- Semi R&D growth
- Demand for new designs, new devices
- Increasing complexity requiring new, advanced solutions

Share Growth Drivers

- Leading expertise and experience in advanced processes and key IP
- Most powerful tools and most complete flows providing better results, lower total cost
- New products/technologies

* This multi-year objective is provided as of December 3, 2014 and is not being updated at this time
Growth in IP/Software Solutions

• 26% of current revenue; 12% trailing twelve-month revenue growth*
• Estimated long-term organic revenue growth: generally in the low double-digits**
• Top-20 semiconductor vendors continue to outsource more IP to Synopsys
• System Design outsourcing driven by need for earlier, more efficient software development, and hardware/software verification

Key Technologies

Interface IP
Analog IP
System-Level Design
Embedded Memories

IP Subsystems
Virtual and FPGA-based prototyping
Software quality, test and security solutions

* As of December 2014
** This multi-year objective is provided as of December 3, 2014 and is not being updated at this time
**#2 IP Vendor**

*Leader in Interface, Analog & Memory IP*

Leadership Enables Investment in Quality, Support, Features and Processes

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### Design IP Revenue, Worldwide (in Millions)*

**Rank** | **Company** | **2013** | **Share**
--- | --- | --- | ---
1 | Synopsys | 193.3 | 43.5%
2 | Silicon Image | 49.1 | 11.0%
3 | Cadence | 44.9 | 10.1%
4 | Rambus | 34.3 | 7.7%
5 | ARM Holdings | 20.2 | 4.5%
6 | L&T Infotech | 11.9 | 2.7%
7 | Arasan Chip Systems | 9.7 | 2.2%
8 | Faraday | 8.3 | 1.9%
9 | PLDA | 7.9 | 1.8%
10 | Mobiveil | 5.5 | 1.2%
**Others** | **59.7** | **13.4%**
**Total** | **444.6** | **100.0%**

*Gartner, April 2014

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### Design IP Revenue, Wired Interface

**Rank** | **Company** | **2013** | **Share**
--- | --- | --- | ---
1 | Synopsys | 193.3 | 43.5%
2 | Silicon Image | 49.1 | 11.0%
3 | Cadence | 44.9 | 10.1%
4 | Rambus | 34.3 | 7.7%
5 | ARM Holdings | 20.2 | 4.5%
6 | eMemory Technology | 27.4 | 11.2%
7 | Kilopass Technology | 22.0 | 9.0%
8 | Mentor Graphics | 9.7 | 4.0%
9 | Sidense | 9.2 | 3.8%
10 | NSCore | 6.8 | 2.8%
**Others** | **11.0** | **4.5%**
**Total** | **244.0** | **100.0%**

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### Design IP Revenue, Memory Cells/Blocks

**Rank** | **Company** | **2013** | **Share**
--- | --- | --- | ---
1 | Synopsys | 76.8 | 31.5%
2 | ARM Holdings | 66.3 | 27.2%
3 | eMemory Technology | 27.4 | 11.2%
4 | Kilopass Technology | 22.0 | 9.0%
5 | Mentor Graphics | 9.7 | 4.0%
6 | Sidense | 9.2 | 3.8%
7 | NSCore | 6.8 | 2.8%
8 | eSilicon | 5.9 | 2.4%
9 | Dolphin Technology | 4.6 | 1.9%
10 | MoSys | 4.4 | 1.8%
**Others** | **11.0** | **4.5%**
**Total** | **244.0** | **100.0%**

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### Design IP Revenue, General Purpose Analog & Mixed Signal

**Rank** | **Company** | **2013** | **Share**
--- | --- | --- | ---
1 | Synopsys | 12.0 | 17.7%
2 | Cadence | 6.8 | 10.0%
3 | QualCore Logic | 5.5 | 8.1%
4 | Faraday | 5.4 | 8.0%
5 | True Circuits | 4.5 | 6.6%
6 | Analog Bits | 3.2 | 4.7%
7 | Kaben Wireless Silicon | 3.0 | 4.4%
8 | RFEL | 2.9 | 4.3%
9 | Dolphin Technology | 2.7 | 4.0%
10 | Silicon Creations | 2.1 | 3.1%
**Others** | **19.7** | **29.1%**
**Total** | **67.8** | **100.0%**

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*Gartner, April 2014

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© Synopsys 2014
Third-Party IP – Synopsys Differentiator

Established Provider
15+ years of investment and execution

Resource Commitment
~2,500 IP Engineers Worldwide

Trusted IP Supplier
Broad portfolio of high-quality, production-proven IP

* Small boxes are standard cell library elements
3<sup>rd</sup> Party IP Usage Will Continue to Double Through 2017

Strong Growth in 3<sup>rd</sup> Party IP Usage

Source: Gartner, March 2013

Percentage of 3<sup>rd</sup> party IP blocks used in SoC design
IP Market Growing to $3.5B by 2017

Source: Gartner April 2013
IP Business Models

**Single Use**
- Customer buys IP for a specific project
- Revenue recognized up front

**Multi-Use Agreement**
- Customer buys a pool of IP that can be used over a multi-year period until the pool is exhausted or the contract expires
- Revenue recognized over time

**Engineering Service**
- Customer pays for porting IP to specific semiconductor process or customization work
- Revenue recognized primarily on % of completion basis
IP Accelerated augments broad, silicon-proven DesignWare IP portfolio with:

- IP prototyping kits with reference designs work out-of-the-box for immediate productivity
- IP software development kits enable early SW bring-up, debug and test
- Customized IP subsystems reduce integration cost, lower risk and speed time-to-market
System-Level Design

• #1 provider of system design solutions including tools, models and services for:
  – Accelerating software development
  – Hardware/Software integration
  – System validation

• Immense chip/system complexity requires new approaches to HW/SW and system integration challenges

• Exploding software content; need more efficient embedded SW development process
Synopsys Enters Software Quality and Security Market with Coverity Acquisition

Coverity Improves Code Quality and Security, Resulting in Better Software, Faster

MOUNTAIN VIEW, Calif. and SAN FRANCISCO, Feb. 19, 2014 /PRNewswire/ -- Synopsys, Inc. (Nasdaq:SNPS), a global leader providing software, IP and services used to accelerate innovation in chips and electronic systems, and Coverity, the leading provider of software quality, testing, and security tools, today signed a definitive agreement for Synopsys to acquire Coverity. Coverity products reduce the risk of quality and security defects, which can lead to the catastrophic failures that plague many of today's largest software systems.

Under the terms of the definitive agreement, Synopsys will pay approximately $375 million, or $350 million net of cash acquired. In addition, Synopsys will assume certain unvested stock options of Coverity employees.

The transaction will be funded by Synopsys with a combination of U.S. cash and debt, and is subject to Hart Scott Rodino regulatory review and other customary closing conditions. The acquisition is expected to close in Synopsys' fiscal Q2.

"Working together, Synopsys and Coverity intend to bring the software development process to the level of 'first-time-right' functionality that software design teams are striving for. For Synopsys this is a natural technology adjacency and the opening of a significant new, growing market space."

Aart de Geus
Chairman and co-CEO, Synopsys

• Acquired Coverity for $375M ($334M net of cash acquired)
• Leading provider of Software Quality, Testing and Security Tools; has averaged ~20% revenue growth
• ~$500M market, expected to grow to ~$1B by 2017
• Natural adjacency and expansion of our TAM; LT growth opportunity beyond our existing customer base, in a fast-growing market we don’t address today
• Funded with U.S. cash plus ~$200M debt
$500M Market Today, Growing ~20%

Synopsys Is Now the Market Leader

Software Quality Analysis and Measurement Market

Software tools to observe, measure, and evaluate software complexity, size, productivity and risk.

Source: IDC (2012)
Current Synopsys Customers
Plus Brand New Customer Base

Current Semis/Systems Customers

- Different Users, Different Budgets

New Verticals, Customers

- Banking, Financial Services, Energy, Aerospace/Defense, Software, Internet, Industrial, etc.

Naturally adjacent
Core competencies:
- Algorithm-based technology
- Some overlapping customers
- Shared high-tech
- Customer-obsessed DNA

New industries Synopsys doesn’t touch today
Synopsys: The Market & Technology Leader

Uniquely Positioned for Stability and Growth

- Dynamic markets
- Clear technology leadership
- Financial strength and growth
Growth and Predictability

- Predictable, time-based revenue model
- Entered FY15 with ~80% of revenue in hand
- Non-cancellable backlog: $3.5B 3-yr backlog end of FY14
- FY14 NG EPS includes the dilution from Coverity

* These targets were provided by Synopsys as of December 3, 2014, and are not being updated at this time
Predictable Time-Based Revenue

- Significant Non-cancellable 3-year Backlog
  - $3.5B at end of FY14
  - More backlog than next 2 largest EDA players combined

- Predictable, time-based revenue model
  - In Q404, began transition to almost fully time-based license model; completed in Q407
  - Orders that once would have been taken to revenue immediately, instead contribute to backlog
  - Revenue recognized over the life of the contract (expecting weighted avg. contract duration of ~3 years in FY15*)

* These targets were provided by Synopsys as of December 3, 2014, and are not being updated at this time
Strong Operating Cash Flow

- Roughly tracks EBITDA less cash taxes over time
- OCF is lumpy
  - Difficult to forecast period to period
  - Timing of large contracts
  - Disbursements (affected by M&A)
- Goal is to optimize the use of our strong cash flow, through a balance of M&A, debt reduction and stock buybacks

* These targets were provided by Synopsys as of December 3, 2014, and are not being updated at this time
Efficient Resource Management

- Most profitable ($) in EDA
- Have reduced G&A and S&M spending (as % of revenue)
- Expect to maintain NG R&D spend at ~30% of revenue
- Goal is to focus on global operational efficiency to deliver solid NG operating margin in the mid-20s range
Technologically & Geographically Diversified

- **Product Groups** (TTM Revenue Growth*)
  - Core EDA: 4%
  - IP & Software Solutions: 12%
  - Manufacturing: -2.5%

- **Geographies** (TTM Revenue Growth*)
  - North America: 7%
  - Europe: 0%
  - Japan: -10%
  - Asia Pacific: 13%

* As of December 2014
Capital Allocation Strategy

Disciplined resource management and allocation

Actively explore TAM-expanding R&D and M&A opportunities

Optimize the use of our strong cash flow, through a balance of M&A, debt reduction and stock buybacks
Solid Balance Sheet

- $911M net cash at end of Q414
- Split of U.S. vs. non-U.S. cash can influence investment decisions
- Buybacks and debt repayments funded entirely with U.S. cash
- Typically like to hold a minimum of ~$100M in U.S. cash on the balance sheet
Returning Cash to Shareholders

- Over the last 5 years, spent $925M on buybacks
  - Purchased 3.1M SNPS shares for $120M in FY14
- $380M remaining on our current share repurchase authorization*
- Goal is to optimize the use of our strong cash flow, through a balance of M&A, debt reduction and stock buybacks

* As of December 2014
Long-term Operating Model*

Primary long-term objective is to drive high-single-digit EPS growth through a mix of the following elements:

- Organically grow traditional EDA revenue generally in the low-to-mid single digit range
- Organically grow IP and Software Solutions revenue generally in the low double-digits
- Actively explore TAM-expanding R&D and M&A opportunities
- Focus on global operational efficiency to deliver solid non-GAAP operating margin in the mid-20s range
- Optimize the use of our strong cash flow, through a balance of M&A, debt reduction and stock buybacks

Note: While the combination of elements may vary, based on business cycles and in-period priorities, our long-term driving principles remain consistent.

* This multi-year objective is provided as of December 3, 2014 and is not being updated at this time
Summary

• Dynamic markets
  – World’s leading EDA supplier and #2 IP vendor

• Clear technology leadership
  – Broadest portfolio of best-in-class technology

• Financial strength and growth
  – Excellent financial position and execution
Thank You