Performance Estimation of Carbon Nanowall-based Field Effect Transistor by 3D Simulation Study

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***Abstract*—We have developed techniques for localized standing vertically Carbon Nanowall (CNW) manufacturing as well as for the methods of controlling their electrical properties. CNW is a bundle of domains consisting of nano graphenes and the thickness of CNW is several nanometers. By incorporating this material in the channel we have proposed new device structure for future generations of CMOS technology. Device electrical parameters have been evaluated by 3D TCAD simulation study. Reliability of the simulated data has been provided by defining new material file based on the realistic parameters modified from the data for Graphene nanoribbon (GNR). Simulation results shown in this paper lead to the conclusion that device performance can be improved by widening the graphene energy bandgap.**

I. Introduction

Starting from 1971 up to now unprecedented integrated circuits scaling down can be observed. A related challenge is to sustain scaling of CMOS logic technology to and beyond 16 nm [1]. Although Intel remains on the Moore's Law pace in terms of constant gate-pitch scaling, with an 112.5nm pitch [2], shrinking is no longer delivering the speed improvements seen in past generations. One approach to sustaining performance gains as CMOS scaling matures in the next decade is to replace the strained silicon MOSFET channel with an alternate material offering a higher quasi-ballistic carrier velocity and higher mobility than strained silicon. Candidate materials include strained Ge, SiGe, a variety of III-V compound semiconductors, and carbon-based materials such as carbon nano tubes (CNTs), graphene, and graphene nanoribbons (GNRs).

II. Nano Carbon-based Field Effect Transistor

The primary potential advantages of Carbon Nanotube FETs are the high mobility of charge carriers and the potential to minimize the subthreshold slope (i.e., minimize the short channel effects) by a surround gate geometry. In the past two years, a recently developed CNT FET compact model [3] projects an ideal 25-50x time increase in switching speed over 32nm CMOS, but only a 2-10x time improvement when parasitic resistances and capacitances are included in practical circuits. On the other hand, there are multiple challenges to achieving this, including: 1) the ability to control bandgap, 2) growth of the nanotubes in required locations and directions, 3) control of charge carrier type and concentration, 4) deposition of a gate dielectric, and 5) formation of a low resistance electrical contact. Graphene materials offer the potential of the extremely high carrier mobilities available to CNTs (without the need for controlling CNT chirality), combined with the promise of patterning graphene nanoribbons using conventional processes. Work on graphene field effect transistors (FETs), while still at an early stage, is proceeding at a rapid pace. Since publication of first description of the electric field effect in graphene [4] several device structures with different gate configuration have been developed such as: bottom gating [4], top-gating [5], and dual-gating [6]. However in all cases devices structures are planar (graphene sheet in the channel is parallel to the substrate). Substrate area taken by graphene nanoribbons is large (channel width and length in µm range). On the other hand important problem with graphene for digital applications is its zero bandgap which in turn will result in a very small I_{ON}/I_{OFF} ratio. In order to open up the band gap, devices with graphene nano ribbons with thickness 5nm (or less) have to be built. For planar technology this may be a major roadblock. To address those challenges we are developing new device structure. In our case device is double-gate (for better device control), with Carbon Nanowalls (CNWs) standing vertically on the substrate (device structure similar to the well-known FinFET device). CNW is a bundle of domains consisting of nano graphenes and the thickness of CNW is several nanometers [7]. This unconventional geometry device can potentially deliver high device integration density and power efficiency at good speed.

III. CARBON NANOWALLS

A. *Electrical properties*

Recently nano-carbon related materials have attracted a lot of interest. Especially, attention has been focused on graphene, a two-dimensional (2D) honeycomb structure of carbon. Graphene makes graphite, when stacked in layers, and carbon nanowalls [8, 9], when standing vertically on the substrate (Fig. 1).

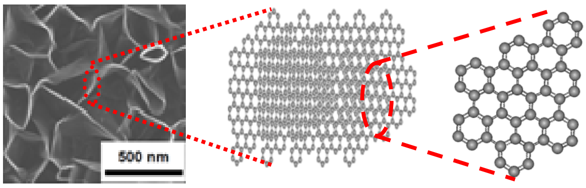

Fig. 1 Top view of Carbon nanowalls (left), graphene sheets (middle), graphene (right).

It has been reported that 2D monocrystalline graphitic films with a thickness of a few atoms exhibit a strong ambipolar electric field such that electrons and holes exist in concentrations of up to $10^{13}cm^{-2}$ and with room-temperature mobilities up to 15000 cm^2/Vs [10]. Carbon nanowalls (CNWs) which are graphene sheets standing vertically on the substrate also possess excellent electrical properties such as: high carrier densities, high carrier mobilities and high sustainable current. Thus field effect transistor with a CNW channel can be a promising candidate for future generation FET devices.

B. *Manufacturing technology*

In order to manufacture CNW film for FET devices we used PECVD technique with radical injection based on a mixture of C_2F_6 with H_2 [11]. Our system consists of a parallel-plate VHF (100MHz) capacitive coupled plasma (CCP) region and a surface-wave-excited microwave H_2 plasma (H_2 SWP) as a remote H radical source. C_2F_6 is introduced into the VHF-CCP region. H_2 is introduced into the microwave SWP region, and H radicals are injected into the VHF-CCP region. The VHF power of the CCP and the microwave power of the SWP can be 270 and 250 W, respectively. Mirror-polished insulating quartz without any catalyst is the substrate used for the growth experiments performed for evaluating the electrical properties of CNW films.

C. *Controlling electrical properties*

We have developed a technique for localized CNWs growth for application in FET device. However for application in CMOS technology we need to able to control CNWs conduction type (*n*-type and *p*-type) as well as its dopant level. Our approach is based on adding a doping gas during CNWs growth process. In order to control the electrical properties of CNWs, additional N_2 gas has to be introduced into the CCP region at flow rates of 1-15 sccm (Table I).

TABLE I. CONTROL OF CNW ELECTRICAL PROPERTIES BY MEANS OF NITROGEN FLOW

N_2 flow rate [sccm]	1	5	10	15
Carrier concentration [$10^{19}cm^{-3}$]	5	8	11	14

CNW manufacturing without any additional gases results in undoped CNW films. The Hall coefficient of the undoped CNW is positive, thus implying *p*-type conduction. In the manufactured CNW films with the N_2 addition it has been observed that the resistivity decreases when the N_2 flow rate increases. The measured Hall coefficient was negative, implying *n*-type conduction (Table II).

TABLE II. HALL COEFFICIENT VS. NITROGEN FLOW

N_2 flow rate [sccm]	1	5	10	15
Hall coefficient [$cm^{-3}C^{-1}$]	-0.13	-0.08	-0.06	-0.04

When adding O_2, we confirmed that it is also possible to control the structure of the CNWs. Oxygen atoms remove impurities thus resulting in highly graphitized CNWs. This is an important issue since the channel graphene layer is responsible for the final device performance. Any impurity can have an effect on static parameters (output current) as well as dynamic operation, i.e. maximum frequency.

IV. FULL 3D TCAD SIMULATION STUDY

Several studies devoted to investigation of GNR-based FET electrical parameters have been presented [12, 13]. However those studies are based on analytical models with number of simplifications and approximations. Excellent device properties can be significantly degraded by adding more phenomena [3]. TCAD study has been also presented [14]. However that study, based on 2D approach, depends on simplified (and ideal) material parameters. When new device is under development intensive modeling and simulation work is required in order to steer experiments. Thus we have decided to perform full 3D study by TCAD approach and to investigate device electrical parameters by incorporating CNW material containing gate dielectric and gate with source and drain.

A. *Material file*

Key issue for reliable qualitative and quantitative analysis is material file. In our research we have used TCAD simulation tool provided by Synopsys and even the latest release is not equipped with material file such as GNR [15]. Thus we defined and added to the application new material. Degradation of electrical parameters of GNR due to Line Edge Roughness has been reported [16]. Change of electrical parameters when ribbons are cut from infinite graphene sheets has been also stated [17]. Thus in order to ensure simulation data reliability we decided to define CNW material file using degraded and cut GNR (Table III) (typical GNR width used during simulations is 5nm).

TABLE III. GNR MATERIAL FILE PARAMETERS IN SENTAURUS

Parameter	Value	Unit	Reference	Sentaurus denotation
E_g	0.32	eV	[18]	Eg0
n_i (5nm)	$1x10^{12}$	cm^{-2}	[14]	ni
μ_e	2000	cm^2/Vs	[16]	mumax
ε	2.5	-	[19]	epsilon
χ	4.5	eV	[20]	Chi0
ϕ	4.66	eV	[21]	*Barrier

*The GNR work function has been defined as the metal–semiconductor work function difference (Barrier) in file defining electrical stimulation conditions.

In the material file, mobility for holes has been assumed the same as for electrons. The effective densities of states in conductance and valence bands have been assumed equal and derived basing on intrinsic concentration value.

B. Device strucure

Device structure shown on Fig. 2 has been investigated by means of device simulations [15]. Standing vertically playing role of channel CNW is grown on SiO_2 (SOI) substrate. At both ends channel is terminated with silicon source and drain (undoped). Gate is separated from source and drain by nitride spacers. Channel (undoped with deposited hard mask) is wrapped with gate dielectric (1nm, HfO_2) and metal gate (Tungsten) thus forming double gate device. This structure is targeted to be feasible in CMOS technology.

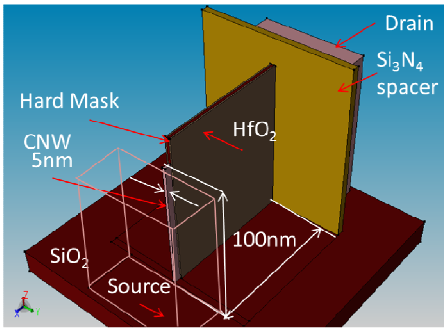

Fig. 2 Idea of FET device based on manufactured GNR.

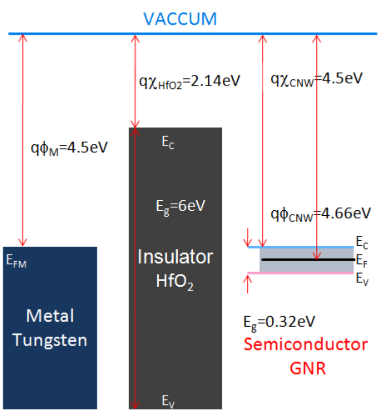

Fig. 3 Band structure of tungsten gate-insulator-GNR (separated).

Material (suitable for *p*-type as well as *n*-type devices) for gate has been tuned to threshold voltage (V_T). Tungsten work function (ϕ) 4.5eV (compared to Al=4.1eV, Ti=4.33eV. Au=5.27eV) is near to GNR mid-gap (intrinsic) energy 4.66eV (Fig. 3). Thus influence of flat-band voltage (V_{FB}) on V_T can be minimized. Tungsten is a refractory metal and good for processing in high temperature process when thermal budget is an issue.

V. RESULTS AND DISCUSSION

Electrical behavior of device has been calculated using drift-diffusion (DD) model (including tunneling effects). Transport mechanism description in GNR is still in development and in its present state contains a number of uncertainties. Even so we believe that the drift-diffusion model approach has a value for design and optimization.

Device simulated transient (I_D-V_{GS}) characteristics for different drain-source potential are shown in the Fig. 4. Source and substrate are grounded whereas gate voltage changes from -1V to 1V and drain potential is 0.05V, 0.2V, 0.5V respectively. Increasing drain-source voltage has led to transconductance increase by nearly factor 4 (from $4.3{\cdot}10^{-9}$S to $1.7{\cdot}10^{-8}$S) but also I_{ON}/I_{OFF} ratio degradation from factor 6 to 3.6 and threshold voltage increase from value -0.28V to -0.36V respectively.

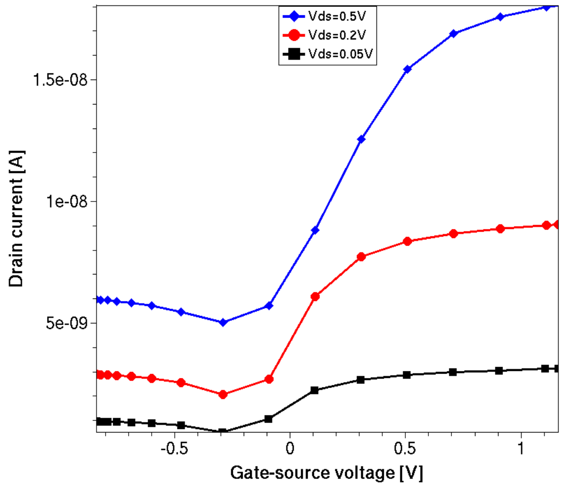

Fig. 4 Calculated I_D-V_{GS} characteristics as function of V_{DS}.

Independently from drain-source voltage for all gate polarization conditions we can observe practically the same order of drain current and the low I_{ON}/I_{OFF} ratios in result. Device is always in on state. For such device to be practical, it obviously needs to turn off when a sufficiently negative bias is applied to the gate electrode.

A. Effect of bandgap

Ideal graphene FET devices have small on/off current ratios because of their lack of bandgap. Widening bandgap leads to better device performance (Fig. 5). In our case increase of transconductance (g_M) (from $4.3{\cdot}10^{-9}$S to $5{\cdot}10^{-9}$S) as well as I_{ON}/I_{OFF} ratio (from 6 to nearly 11), has been obtained when changing E_g from 0.32eV to 0.96eV. Subthreshold swing decrease can be also observed.

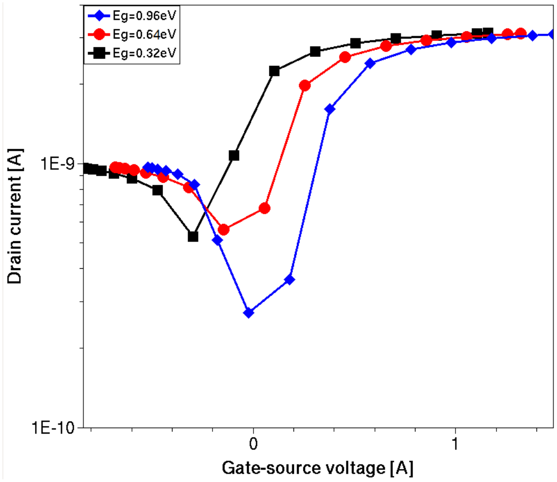

Fig. 5 Calculated I_D-V_{GS} characteristics as a function of E_g.

Bandgap had little effect on the on-state current whereas the off-state current (at negative gate voltage) is largely associated with band-to-band tunneling.

VI. Conclusions

New device structure with Carbon Nanowall (CNW) channel has been proposed in this paper. By defining new material file we presented an approach for device performance modeling and optimization. It has been shown that CNW consisting of cut graphene nanoribbons (which inherently possess edge roughnesses) leads to device electrical parameters (i.e. g_M, I_{ON}/I_{OFF} ratio) degradation when applied in the channel. Device performance has been improved by energy bandgap widening. Further device performance improvement can be obtained by source and drain doping level tuning thus forming tunneling Schottky junction with the CNW channel.

It is still unclear whether or when graphene (in any form) will be introduced to practical electronics technology however developing device-oriented theory for device design and optimization is required.

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