Analysis of threshold voltage variations of FinFETs relating to short channel effects

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Introduction

Double-gate MOSFETs, such as FinFETs, are candidates for future short channel MOSFETs because of their superior gate control to that of conventional planar MOSFETs [1]. Variation of threshold voltage (*Vth*) which appears with down sizing of devices is identified as a serious problem [2,3], however, it has not been studied so systematically for FinFETs comparing to the planar MOSFETs. In this paper, we evaluated the variation of *Vth* of FinFETs originated form deviations of various parameters of device size and impurity concentration by 2D device simulator, and revealed that there exist different origins, those related with short channel effects (SCEs) and those unrelated to SCEs. The effect that these two origins cancel out each other was found to suppress the *Vth* variation, and it appeared under different conditions for the FinFETs and the planar MOSFETs

Simulations and Results

Simulated device models and parameters are shown in Fig.1 and Table 1. Gate length (*Lg*) and EOT are identical for the planar MOSFETs and the FinFETs. Two different values of channel doping concentration (*Nc*) are employed for the FinFETs, such as $Nc = 8.1 \times 10^{18}$ cm^{-3} for "FinFET-I", $Nc = 1.0 \times 10^{17}$ cm^{-3} for "FinFET-II" and $Nc = 10^{15}$ cm^{-3} for "FinFET-III" with underlap [4] while, only $Nc = 8.1 \times 10^{18}$ cm^{-3} is employed for the planar MOSFETs. As well as these short channel devices, the long channel devices (*Lg*=1.0 μm) having another parameters identical to those of the short channel devices were used in order to extract factors relating to SCEs. On these devices, *Vth* shifts for 10% increase in structural parameters such as *Lg*, Fin width (*Wfin*), *Nc* and EOT were evaluated. And a difference between the obtained value for the short channel device and that for the long channel device was derived as a factor related with SCEs for each evaluation.

Obtained results are shown in Fig. 2. For the *Lg* deviation, the *Vth* variations of the short channel devices are fully originated from SCEs. The FinFET with low *Nc* leads lower *Vth* variation than that with high *Nc*. For the *Wfin* deviation, interesting phenomenon is observed. *Vth* variation for short channel FinFET with high *Nc* is much smaller than that with low *Nc* in FinFET I and FinFET II. However, the small *Vth* variation is resulted from cancellation out between the factor of SCEs represented by the difference described above and that independent of SCEs represented by the long channel. In FinFET III, as *Leff*(OFF) > *Lg* in weak inversion, *Vth* variation is smaller than other FinFETs used in this work. For the *Nc* deviation, the *Vth* deviation of the FinFET with low *Nc* is very small. For the EOT deviation, signs of *Vth* variation are opposite for the planar MOSFET and the FinFET I and FinFET II, and the significant cancellation effect is observed for the planar MOSFET. However, in FinFET III, *Vth* variation due to EOT variation is smaller due to better short-channel performance.

Conclusion

In the origins of *Vth* variation of FinFETs for deviation of device parameters such as *Lg*, *Nc*, *Wfin* and EOT, there are two different factors, those related with SCEs and those unrelated to SCEs. For deviation of particular device parameters, cancellation between these two factors having opposite sign each other results in apparent suppression of *Vth* variation. And the deviating device parameters for which such cancellation effects are observed are different for the FinFETs and the planar MOSFETs.

Acknowledgements

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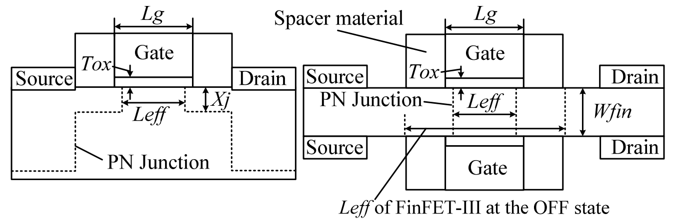

Fig. 1 Simulated device models: (a) Planar MOSFET, (b) FinFET.

Table 1 Device dimensions used in this work.

Gate Length (*Lg*)	16 nm (short channel)
Effective Gate Length (*Leff*)	12.5 nm
EOT (nm)	0.5nm (*Tox* = 2.7nm(HfO_2))
Junction depth (Xj)	5.8nm
Leff of FinFET-III at the off state	36 nm
ε_r of spacer material in FinFET-III	20

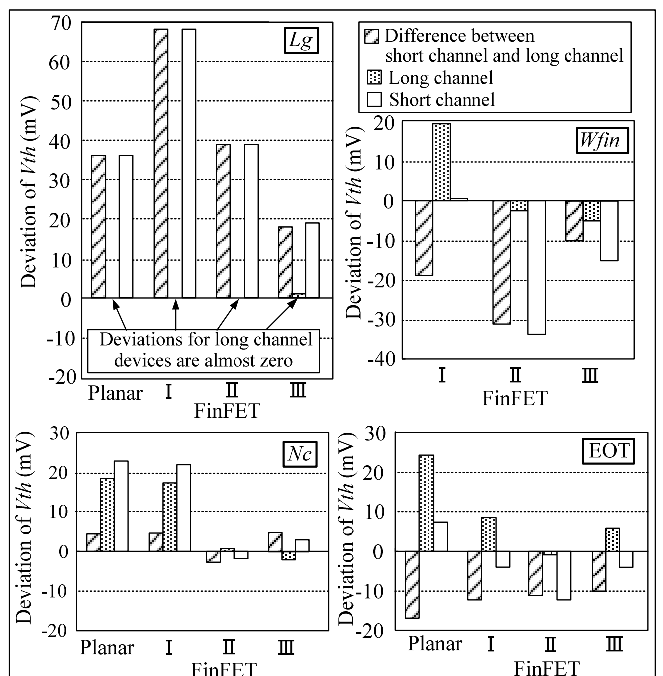

Fig. 2 Deviation of *Vth* of planar MOSFET and FinFETs for +10% deviation of *Lg*, *Wfin*, *Nc* and EOT. $Nc = 8.1 \times 10^{18}$ cm^{-3} for FinFET-I and planar MOSFET, $Nc = 1.0 \times 10^{17}$ cm^{-3} for FinFET-II, and $Nc = 1.0 \times 10^{15}$ cm^{-3} for FinFET-III.