

# Synopsys' Open Educational Design Kit: Capabilities, Deployment and Future

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## Abstract

An open Educational Design Kit (EDK) which supports a 90nm design flow is described which includes all the necessary design rules, models, technology files, verification and extraction command decks, scripts, symbol libraries, and PCells. It also includes a Digital Standard Cell Library (DSCL) which supports all contemporary low power design techniques; an I/O Standard Cell Library (IOSCL); a set of memories (SOM) with different word and data depths; and a phase-locked loop (PLL). These components of the EDK augment any type of design for educational and research purposes. Though the EDK does not contain any foundry information, it allows real 90nm technology with high accuracy to be implemented in the designs.

## 1. Introduction

In the age of nanometer technologies, universities strive to provide the most modern and high quality studies in IC design. In addition to Electronic Design Automation (EDA) tools from leading companies, Educational Design Kits (EDKs) for different IC fabrication technologies are also necessary. But creation of such EDKs is challenged by numerous difficulties such as labor-intensive development and considerable complexity of verification. However, the most important of the challenges are the intellectual property (IP) restrictions imposed by IC fabrication foundries which do not allow universities to copy their technology into EDKs. That is why it became necessary for Synopsys to create an open EDK which on one hand did not contain confidential information from foundries, and on the other hand, has characteristics very close to the real design kits of the foundries.

## 2. Overview of the EDK

Synopsys has created an open Educational Design Kit (EDK) which is free from intellectual property restrictions and is targeted for educational and research purposes. It is aimed at programs for training highly qualified specialists in the area of microelectronics at different universities, training facilities, and research centers. The EDK is intended to support the trainees so

they can better master today's advanced design methodologies and the capabilities of Synopsys' state-of-the-art IC design tools. It allows students to design different ICs using 90nm technology and Synopsys' EDA tools. It also gives them the ability to practice current methods of low power design.

The Synopsys EDK contains the following: a technology kit (TK), a Digital Standard Cell Library (DSCL), an I/O Standard Cell Library (IOSCL), a set of memories (SOM), and a phase-locked loop (PLL).

For the EDK's development, an abstract 90nm technology was used. While the EDK does not contain actual foundry data, which is confidential information from foundries, it is very close to real 90nm technology. Using the abstract 90nm technology allowed Synopsys to create an open EDK which can be used for study and research of real 90nm design characteristics.

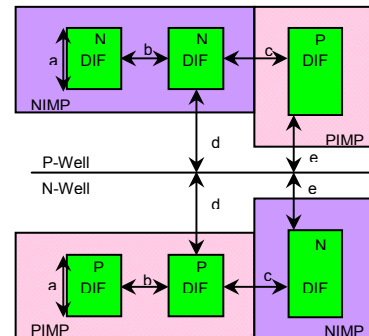
## 3. Description of the EDK components

### 3.1. Technology Kit

The technology kit (TK) is a set of technology files needed to implement the physical aspects of a design. The generic TK for education contains:

1. Design Rules. These rules were created by using the MOSIS Scalable CMOS (SCMOS) design rules. They provide greater portability of designs than if 90nm rules were developed because the sizes in 90nm rules can be larger by 5-20% than those in real foundry processes.

An example design rule is illustrated in Figure 1.



a=0.12, b=0.14, c=0.18, d=0.24, e=0.2um

Figure 1. Example Design Rule

2. Device Formation. This portion of the TK contains the description of available devices and their layout

formation rules. It represents all the devices offered in the 90nm 1.2v/2.5V generic process.

Figure 2 illustrates examples of device formation.

3. GDSII Layer Map. This part of the TK contains layer names and GDSII numbers used in the 90nm process. Some layers such as dummy, marking, and text, have been added to the MOSIS layer map. Any layer numbers may be chosen to form a generic process. A sample of the layer map is shown in Table 1.

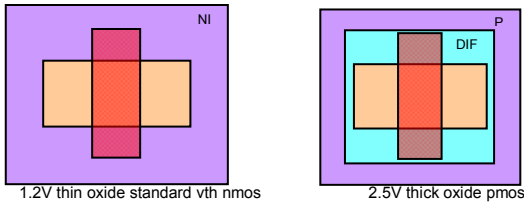


Figure 2. Examples of Device Formation

4. Process Description. This section of the TK provides approximate values of dielectric and metal thicknesses.

Table 1. Sample of Layer Map

Layer #	Data type	Tape Out Layer	Drawing or Composite Layer	Layer name in TechMap File	Layer Name in DRC	Layer Name in LVS	Layer usage description
1	0	YES	Drawing	NWELL	NWELLI	NWELL	NWELL
2	0	YES	Drawing	DNW	DNWi	DNWi	Deep NWELL

5. Generic SPICE model library. These are based on the Predictive Technology Model [1]. The SPICE model library contains the following devices:

- transistors
  - a) 2.5V devices: thick oxide MOSFETs
  - b) 1.2V devices: thin oxide MOSFETs with typical, high, and low threshold voltages. Each of these devices have five corner models: TT - both typical; FF - both fast; SS - both slow; SF - slow nmos/fast pmos; FS - slow pmos/fast nmos.
- diode
- unalicyded P+ poly resistor

In order to estimate the accuracy of the SPICE models, the models' parameters were scaled to 0.25um technology to compare them with the characteristics of known 0.25um models (Figure 3). A set of DC transfer curves was obtained and the middle curve from the set was chosen as a typical corner for 2.5V devices, thereby assuring that it is close to the real foundry process

FF, SS, SF and FS corner models were formed by changing the threshold voltage (vth0) and oxide thickness (tox) in the range of +/-5%. Figure 4 shows the transfer curves for TT, FF and SS corners of a thick oxide NMOS model.

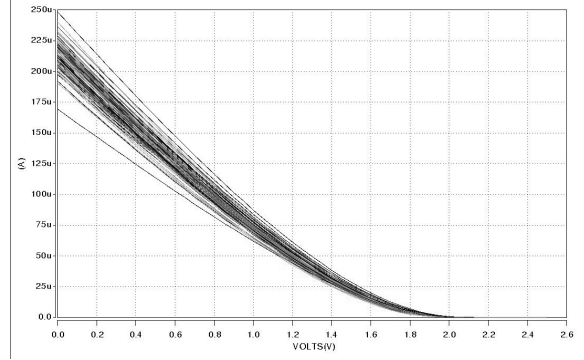


Figure 3. Set of .25um Transfer Curves

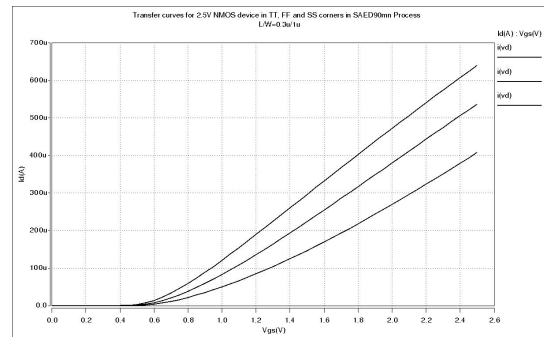


Figure 4. TT, FF and SS corners of 2.5V thick oxide NMOS

6. Milkyway technology file. This file contains rules used by Synopsys' EDA tools.

7. Generic symbol library and PCells. The generic symbols and PCells in this library are: MOS transistors, resistors, BJTs, and diodes. The PCells were developed using the TCL scripting language to work in Synopsys' Cosmos Schematic Editor environment.

8. DRC and LVS rule decks. These are the design rules needed for Synopsys' Hercules tool to perform design rule checks and layout vs. schematic.

9. Extraction files. These are files used by the Synopsys Star-RCXT tool for parasitic extraction: ITF, TLU+, mapping, and command files.

10. Support scripts. A variety of additional scripts are required to support the design flow. For example, a script for converting a SPICE generic netlist to the given technology and PCell setup scripts.

### 3.2. Digital Standard Cell Library

The Digital Standard Cell Library (DSCL) is used for designing different ICs in 90nm technology with Synopsys' EDA tools. The DSCL was built using 1P9M 1.2V/2.5V design rules and is aimed at optimizing the main characteristics of an IC design.

The DSCL contains a total of 251 cells. The library includes typical combinational logic cells with different drive strengths.

The library also contains all the cells which are required for different styles of low power designs [2]. These cells enable the design of ICs with different core voltages to minimize dynamic and leakage power (clock gating cell w/ latched pos edge control post, pre, non-inverting delay line - 0.5-2.0 ns; pass gate; bi-directional switch w/ active-low enable; hold 0 isolation cell - logic AND; hold 1 isolation cell - logic OR); low-to-high level shifter; high-to -low L=level shifter; pos edge retention DFF w/ async active-low reset; scan pos edge retention DFF w/ async active-low reset; neg edge retention DFF w/ async active-low reset; scan neg edge retention DFF w/ async active-low reset; header cell; footer cell; always on non-inverting buffer, etc).

The DSCL also contains miscellaneous cells that complete the library. Composite Current Source (CCS) modeling technology was used for cell characterization to meet the requirements of contemporary low power design methods. CCS provides timing, noise, and power analyses while considering the relevant nanometer dependencies. CCS allows the requirements of variation-aware analysis to be met.

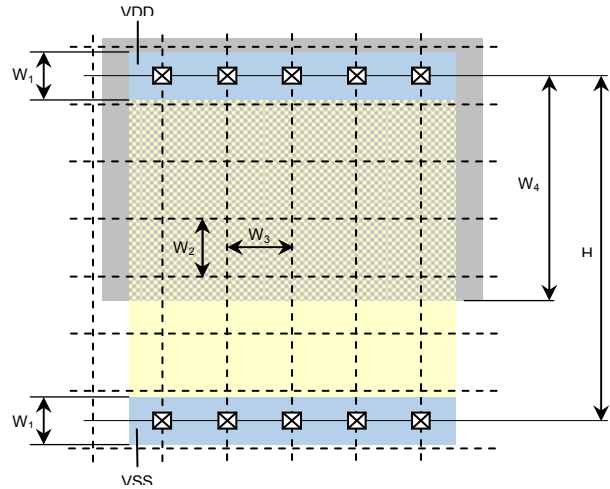
In order to fully meet the requirements of low power design techniques, the DSCL was characterized for the 16 process/voltage/temperature conditions shown in Table 2.

**Table 2. Characterization Conditions**

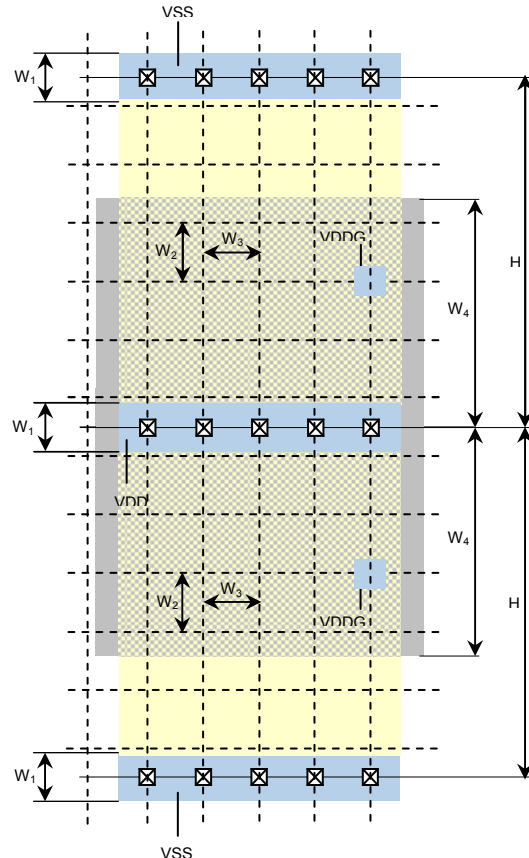
Corner Name	Process (NMOS proc. - PMOS proc.)	Temperature (°C)	Power Supply (V)
FFHT1p32v	Typical - Typical	25	1.2
TTHT1p20v	Typical - Typical	125	1.2
TTNT1p20v	Typical - Typical	-40	1.2
FFLT1p32v	Slow - Slow	25	1.08
SSHT0p07v	Slow - Slow	125	1.08
TTLT1p20v	Slow - Slow	-40	1.08
SSLT0p07v	Fast - Fast	25	1.32
FFNT1p32v	Fast - Fast	125	1.32
SSNT0p07v	Fast - Fast	-40	1.32
SSLT1p08v	Typical - Typical	25	0.8
SSNT1p08v	Typical - Typical	125	0.8
SSHT1p08v	Typical - Typical	-40	0.8
TTHT0p08v	Slow - Slow	25	0.7
TTNT0p08v	Slow - Slow	125	0.7
TTLT0p08v	Slow - Slow	125	0.7
FFHT0p90v	Slow - Slow	125	0.7
FFNT0p90v	Fast - Fast	125	0.9
FFLT0p90v	Fast - Fast	-40	0.9

Functionality of the DSCL was also checked at many additional simulation conditions. The DSCL has all the necessary deliverables.

The selection of the physical structure of the digital cells was made to provide maximum cell density in digital designs as well as to take into consideration the requirements of low power design techniques. That is why single (Figure 5) and double (Figure 6) height structures have the parameters which are shown in Table 3.



**Figure 5. Physical structure of single height cells**



**Figure 6. Physical structure of double height cells**

**Table 3. Physical structure dimensions**

Parameter	Symbol	Value
Cell height	H	2.88 $\mu\text{m}$
Power rail width	$W_1$	0.16 $\mu\text{m}$
Vertical grid	$W_2$	0.32 $\mu\text{m}$
Horizontal grid	$W_3$	0.32 $\mu\text{m}$
NWell height	$W_4$	1.68 $\mu\text{m}$
VDDH to VDDL height (Fig. 8.3)	$W_5$	0.72 $\mu\text{m}$

### 3.3. I/O Standard Cell Library

The I/O Standard Cell Library (IOSCL) is used for designing different integrated circuits (ICs) in 90nm technology using Synopsys' EDA tools. It was built using 90nm 1P9M 1.2V/2.5V design rules developed by the Synopsys Armenia Educational Department (SAED).

Providing a complete set of standard functions, the IOSCL contains 36 cells (including CMOS non-inverting input buffer; CMOS non-inverting bi-directional cell; 2/4/8/12/16 mA tri-state driver with pull-up and pull-down; analog, non-inverting bi-directional without resistor pad with ESD protection; core power; I/O power; core ground; I/O ground pads; cross-coupling diode; IOVSS to VSS; decoupling capacitors VDD to VSS and IOVDD to IOVSS; break cell; corner pad; filler cell; bonding pad). CCS modeling technology was used for characterization of the IOSCL. All cells are 65 $\mu\text{m}$  x 300 $\mu\text{m}$  in size or smaller.

### 3.4. Set of memories

The set of memories (SOM) was designed using the SAED 90nm 1P9M 1.2V/2.5V process. It includes a set of several static RAMs (SRAMs) with a small number of words (word depth - m) and bits per word (data width - n). All SRAMs included in the SOM are synchronous dual-port SRAMs with write enable, output enable, and chip select on each port. Also included are 16 SRAMs which have the same architecture but different nxm (width x depth) sizes where n=4,8,16,32 and m=16,32,64,118. These synchronous dual-port nxm SRAMs have two ports (primary and dual) for the same memory location. Both ports can be independently accessed for read or write operations.

### 3.5. Phased locked loop (PLL)

The phase-locked loop (PLL) is a clock multiplier circuit that can generate a stable, high-speed clock from a slower clock signal. It was designed using the

SAED 90nm 1P9M 1.2V/2.5V process. The PLL has 3 operating modes: normal, external feedback, and bypass. In the external feedback mode, the feedback input clock is phase-aligned with the input clock. These aligned clocks allow removing clock delay and skew between devices. In bypass mode, the reference clock is bypassed to the output.

## 4. EDK's deployment

The Synopsys EDK is in use for both educational and research purposes. The EDK has been deployed at leading universities around the world including: Syracuse University (New York, USA), University of California Extension (Santa Cruz, USA), Purdue University (Indiana, USA), Oregon State University (Corvallis, USA), California State University, Northridge (Los Angeles, USA), Silicon Valley Technical Institute (San Jose, USA), University of California (San Diego, USA), San Francisco State University (San Francisco, USA), University of Tennessee (Knoxville, USA), Indian Institute of Technology Kanpur (Kanpur, India), Kate Gleason College of Engineering (New York, USA), Rochester Institute of Technology (New York, USA), State Engineering University of Armenia (Yerevan, Armenia), Yerevan State University (Yerevan, Armenia), Russian-Armenian Slavonic State University (Yerevan, Armenia), Moscow Institute of Electronic Technology (Moscow, Russia).

It is also used in a number of training centers including Synopsys' Customer Education Services, Synopsys' Corporate Application Engineering team, and Sun Microsystems.

There are several good examples of how the EDK is furthering education in microelectronics. All the universities included in Synopsys' programs for industry-university collaboration in microelectronics education [3] use a new microelectronics curriculum created by Synopsys, Inc. [4] which is fully based on the developed EDK. This means the curriculum makes use of the EDK for all laboratory exercises, course projects, diploma requirements, Master's theses, and PhD dissertations. Other universities use the EDK in their educational design flows such as University of California Extension, Santa Cruz in its "Advanced Physical IC" course, San Francisco State University's School of Engineering in its "Custom Design Project for VLSI" courses [5], and Oregon State University in its "Network-on-chip Router" project.

For research, the EDK is used for a variety of projects such as those being worked on by Syracuse University PhD students, California State University Northridge graduate students in low power related projects, Sun Microsystems for the OpenSPARC project, and Synopsys' Corporate Applications

Engineering team in their “ChipTop” design for the Unified Power Format (UPF) low power design flow.

## 5. EDK’s future

To keep pace with industry advancements, creation of new EDK versions for 65nm and 45 nm technologies is anticipated. These new versions will be developed with the same techniques, have approximately the same capabilities, but will comprehend design challenges set by 65nm and 45nm technologies. Further additions of cells in the SOM are also anticipated, particularly for memory cells present in well-known designs (for example, OpenSPARC).

## 6. Conclusion

An open Educational Design Kit (EDK) was created and tested by Synopsys. It can be used for educational and research purposes, is free from intellectual property restrictions, and is representative of industrial design kits. It can be used in a wide range of design flows for digital, analog and mixed-signal designs using Synopsys’ EDA tools. The breadth of its deployment in universities and training centers around the world demonstrates that it serves its goals.

## 7. References

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