

# EDA is an Ecosystem: Interoperability and the Future of EDA

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# A Healthy EDA Ecosystem is Essential...

- To the \$256B semiconductor industry\*
- To the \$1T+ electronics industry

# EDA is an Ecosystem

## In a healthy EDA ecosystem...

- Startups innovate new tools
- Big firms acquire/integrate technology into flows
  - Leverage massive sales channels to offer flows to customers
- Flows help customers create designs quickly to
  - Build more chips
  - Buy more tools (hopefully)
- New batch of startups look into next gen challenges

# Growth by Acquisition Model

- Startups historically account for majority of EDA innovations/de facto standards
  - PrimeTime, Physical Compiler, Calibre are some exceptions
  - Healthy startup environment requires venture capital (which requires reasonable ROI)
  - Unhealthy startup environment detrimental to EDA and thus semiconductors, thus electronics
  - Si2 OpenAccess was/is visionary: EDA embraces growth by acquisition model

# Interoperability Essential to Growth by Acquisition Model

- Successful startup environment requires open access to tool formats and foundry data
- Standards “open” but only after lots of drama
  - Verilog & VHDL
  - .lib
  - LEF
  - DEF
  - e/Vera/SystemVerilog/SystemC
- Standards that still are not open
  - SKILL
  - Low Power = UPF/CPF
  - others

# Interoperability is Essential (cont.)

- Industry typically thrives when sharing standards
  - Startups can quickly create tools for new flows
  - Acquiring EDA companies can quickly integrate new tools into existing flows
    - Also reduces EDA R&D
  - Customers can quickly integrate new functionality into existing flows & adopt new ones
    - Faster TTM

# But EDA Ecosystem can Become Unbalanced

- Missteps of big (or small?) EDA company can negatively impact entire ecosystem
- 1999-2000 FAM debacle (seemingly repeated this year)
- Litigations (Cadence v. Avanti, Mentor v. Quickturn, Synopsys v. Magma)
- Buffet licensing
  - Pricing competition equals lesser value for entire sector?
    - “Once you reduce the price of a tool, you can never raise the prices of that tool again”
      - Cadence reduces Ambit to \$25k
- Isolationism
  - “There is no EDA industry--We are the EDA industry”
    - Lack of participation in industry events, Standards bodies, Tradeshow

# Ongoing Challenges to Ecosystem

- ASIC starts continue decline especially on advanced nodes

2000	2005	2006	2007	2008
7,749	3,623	3,408	3,275	3,048*

Questions:

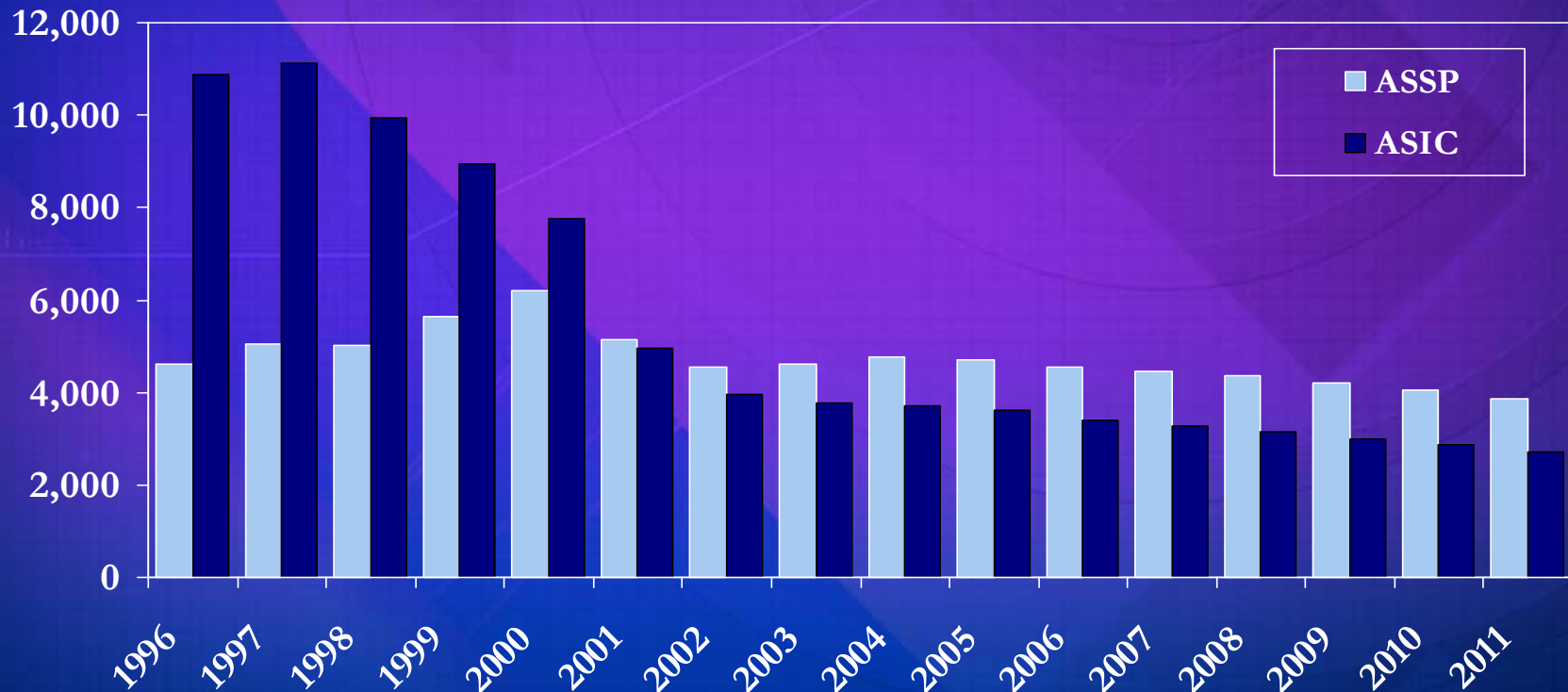
How many of those design starts were successful—actually became products?

How many of those products were successful?

# ASIC & ASSP Design Starts Shrinking

ASIC & ASSP Design Starts (Tape Outs)

Number of Design Starts

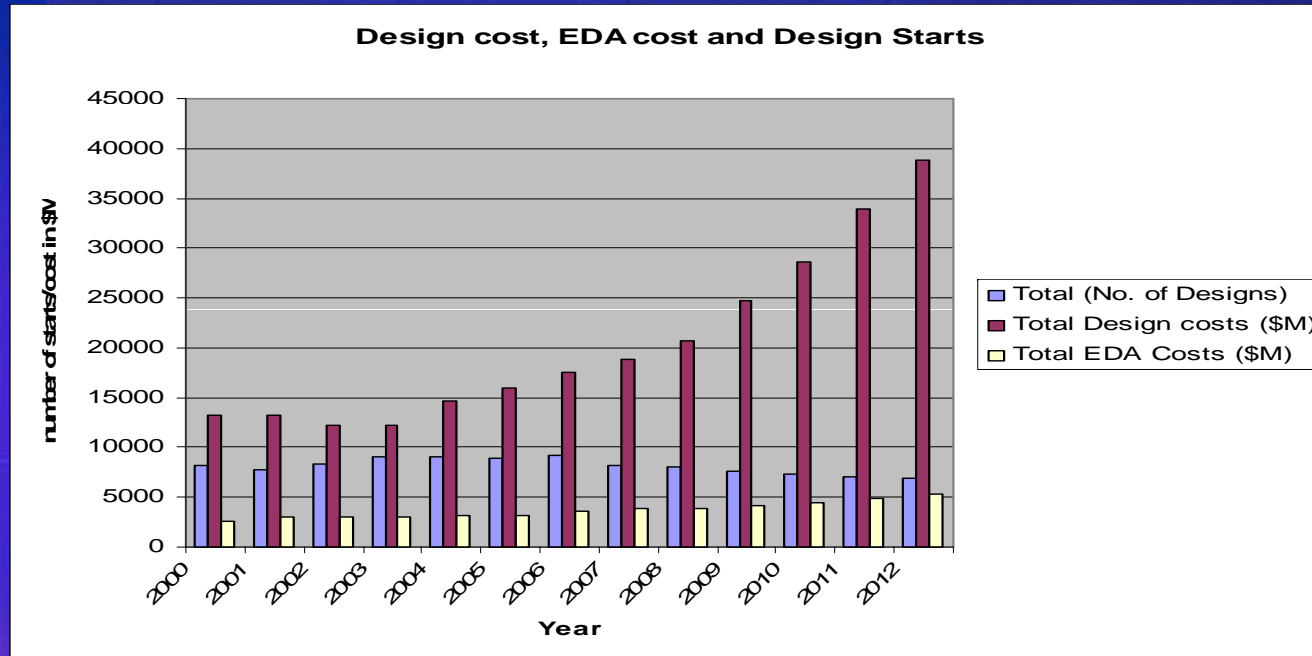


Source: Gartner Dataquest Estimates, 2008

# Complexity and Cost of New Processes Increase

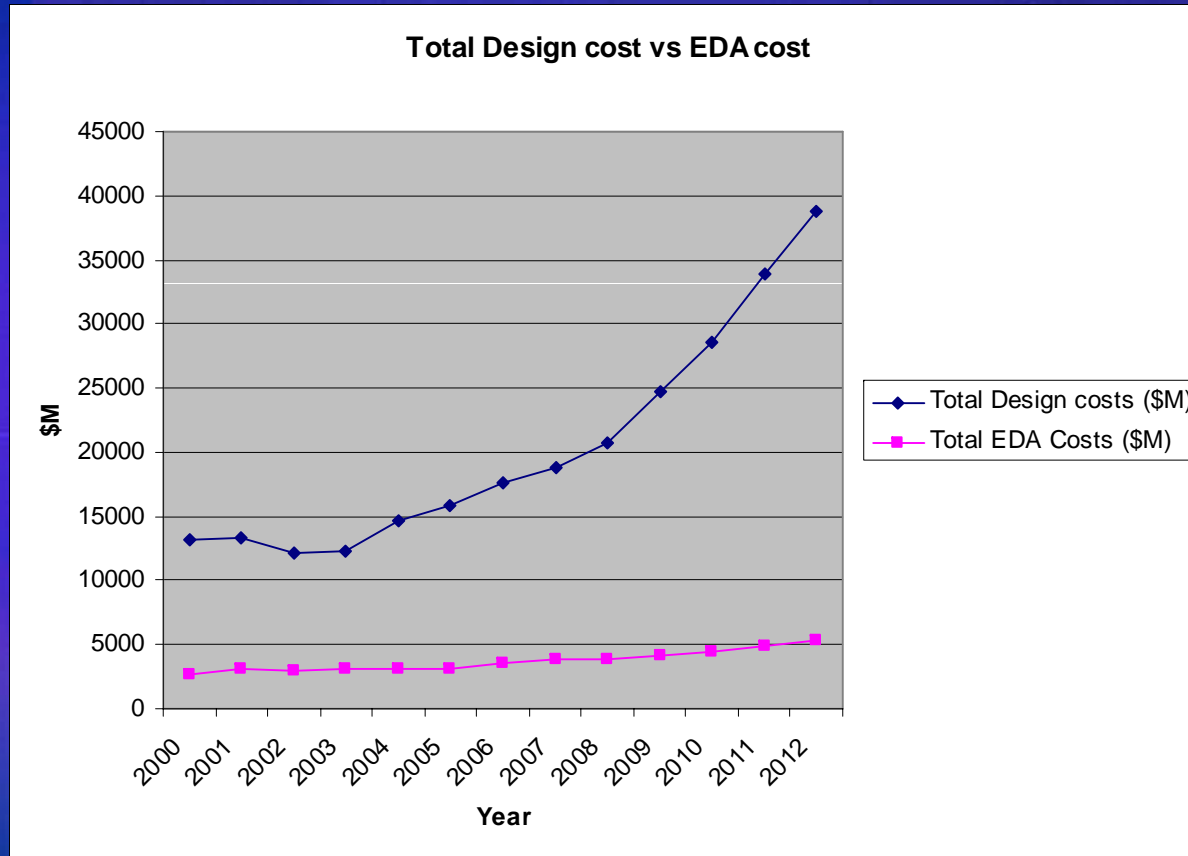
- 45nm leakage accounts for 60+% of power consumption
- Mask set costs exceed \$1 million (30 masks per set)
- Variability/reliability started to show up at 65nm
- Longer design/verification cycles
  - Greater EDA tool expenditure?
    - Greater customer NRE

# EDA Cost Becoming Smaller Percentage of Overall Design Cost...

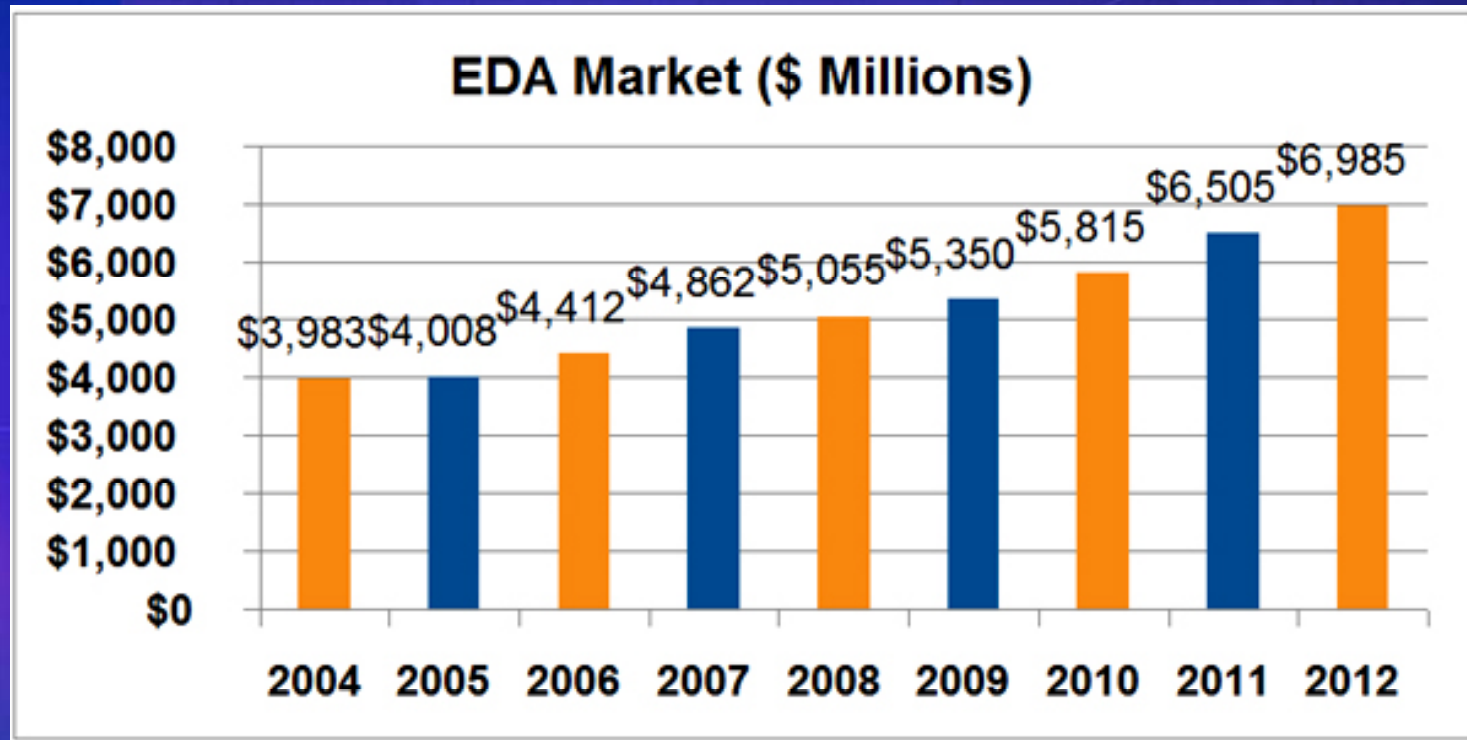


	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
EDA as a % of total costs	20%	23%	24%	25%	21%	20%	21%	20%	19%	17%	16%	14%	14%

# EDA Cost Becoming Smaller Percentage of Overall Design Cost



# More Revenue from Fewer Customers?



*"Gary Smith dispels EDA 'fear, uncertainty, doubt'"*  
By SCD Source, Richard Goering 06/09/08

# Is 2008 Just 2001 All Over Again?

- Economic crisis...recession?
  - Unknown impacts on
    - Semiconductor spending and R&D
    - Already declining ASIC and ASSP starts
    - The EDA ecosystem

# The Last Time we Hit a Recession...

- Semiconductor vendors stopped spending
- 2001 was a good year for EDA—5 of top IPOs across all industries
  - Some EDA spokespeople claimed “EDA was immune to the downturn” – companies must design to innovate out of recession
- EDA vendors experienced delayed effects
  - Learned hard lesson – industry tied closely to semiconductors

# EDA is the Skier Behind the ASIC/ASSP Semiconductor Boat



# EDA Trade News is the Squirrel Being Towed by the Skier



# During the 2001 Downturn

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# 2001 Proved EDA is Not Recession-proof

- In 2001-2002 “companies have to design out of a recession”—wasn’t true
  - Customers made do with tools they already purchased

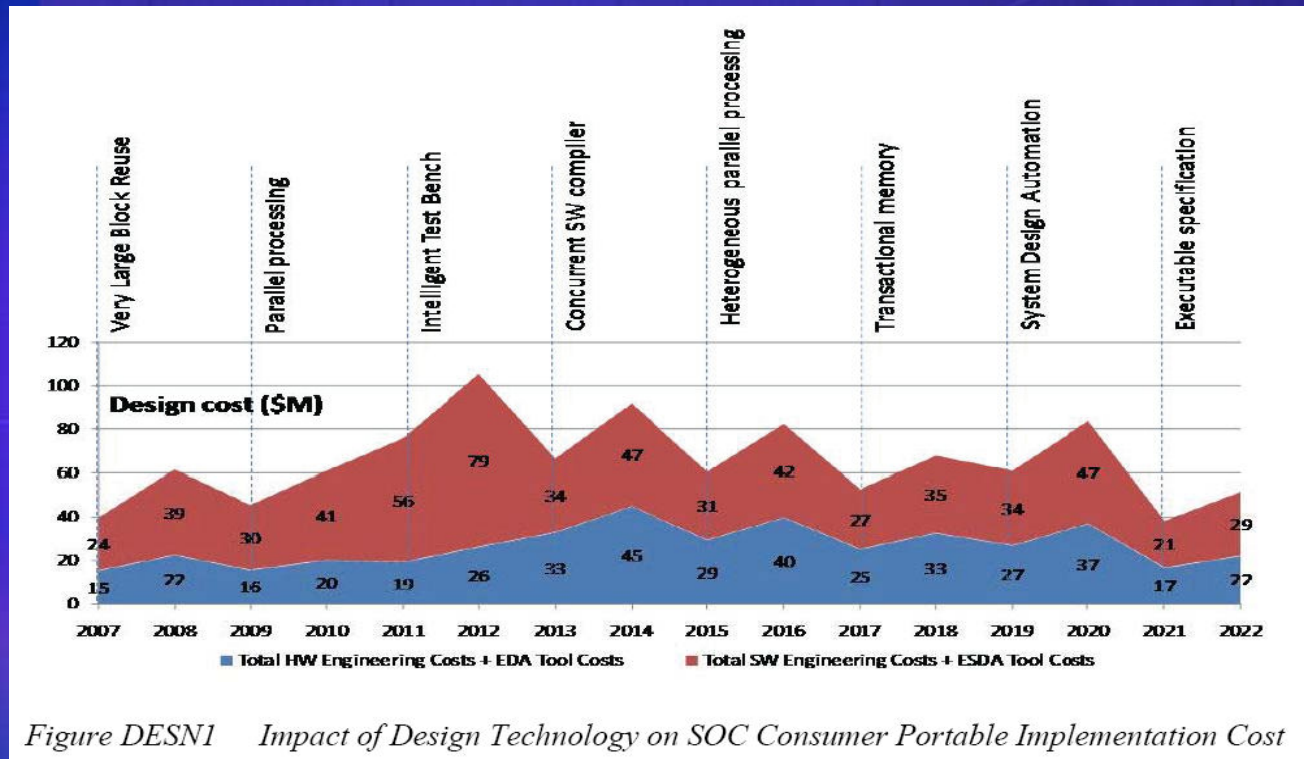
# EDA Innovation is Essential to Building a Better Boat



# Digital Flow Innovation Still Needed

- Many problems still to be solved for advanced silicon processes  
(Xilinx is EDA customers as well as FPGA tool developer)
  - Power management
  - Variability
  - DFM
  - Verification
  - IP for new process geometries
  - ESL?
- Inevitable need for retooling
  - No major retooling since 130nm
  - New retooling for 32nm, maybe 40nm?
  - Do fewer design starts mean fewer customers willing to retool?

# Can't Differentiate with HW; Do it in SW



Electronic System Level Design at DAC'08 – Sunday

Posted by Frank Schirrmeister on June 9th, 2008

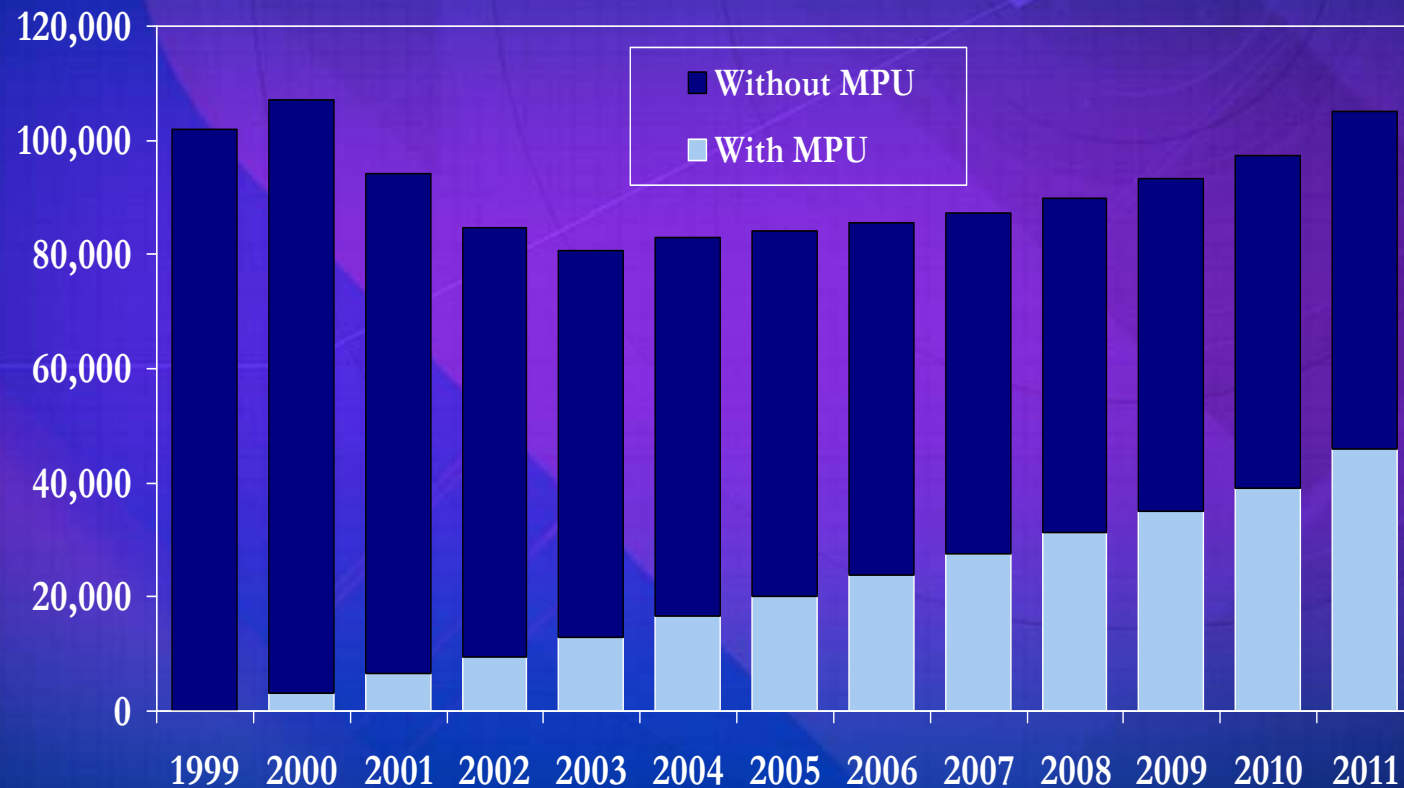
ITRS

# Expand Beyond Digital ASICs

- FPGAs: 55,000+ FPGA total design starts and growing
  - Put EDA ingenuity into FPGA tools, as well as ASSPs
    - FPGAs will be differentiation IC going forward
      - Offer differentiation in HW as well as SW
    - Undeniably growing user base
      - Applications increasing rapidly beyond wired networking
      - Wireless (base stations—Software Defined Radio)
      - Automotive and ISM
      - A&D
      - Even consumer!
  - EDA opportunities in FPGA tool development
    - Hardware/software “RE-programmability”
      - Low power mitigation
      - HW/SW co-design/verification
      - Push button flows—FPGA tools for embedded and algorithm developers
      - Convert familiar ASIC tool flows to FPGA flows
      - IP for new FPGA platforms

# FPGA/PLD Design Starts

Number of Design Starts



# Accelerate Growth Beyond Digital ASICs (cont.)

- Mixed signal ASICs/ASSPs
  - Moore's Law won't scale for most logic designs
    - Expect slower adoption of new processes
    - New twists on mature processes
      - Mainland China
      - Mixed signal
- SiP
  - Two years ago, Samsung released a memory with 22 stacked die

# Interoperability is Essential to the EDA Ecosystem

- Collaborate on standards
- Embrace growth-by-acquisition strategy
- Fund and actively participate in Si2, Accellera—  
re-establish EDA council
- Work with customers
- EDAC establishes revenue recognition guidelines/best  
practices/recommendations (avoid collusion)
- EDAC gets rid of bylaws that say EDAC president  
must be from big public company (new blood)
- Attend DAC

# EDA Industry Needs to Buy into its Own Messaging

- “Where electronics begins!”
- Recognize the innovations you’ve enabled and the lives your technologies have saved...
- Focus on the larger cause—help customers innovate
  - If EDA better serves customers, money and Wall Street will certainly follow

# Entire EDA Industry Must Collaborate for Success

