Design for Low Power

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Power Management

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Power Management Approaches

**Architectural**
- Hardware vs. Software
- Hardware / Software Allocation
- Multi-threshold, Multi-voltage
- Clock, data gating
- Low-power circuits
- Retention latches
- Power aware memories

**System Level**
- Algorithm/Implementation
- Tradeoffs

**Software**
- Compilers
- Power aware OS
- Hibernation modes
- Memory Access

**Hardware & IP**
- Multi-threshold
- Multi-voltage
- Low-power circuits
- Retention latches
- Power aware memories

**Process**
- Multi-threshold, Multi-voltage, SOI, High-K, Body bias, Copper interconnect, SiGe substrates

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Galaxy Power Management

Power Management Throughout the Design Flow

**Power Compiler**
- Dynamic and leakage power optimization within DC & PC
- RTL power analysis

**PrimePower**
- Gate-level peak and average power analysis
- Vector-Free Capability

**JupiterXT**
- Design planning, power network analysis

**Astro-Rail**
- Voltage-drop and electromigration analysis
Power Dissipation In CMOS Designs

Dynamic Power \[ P_{\text{dyn}} = a f^* C * V^2 \]

- Switching Power
  - Load Capacitance
    Charge/Discharge
- Internal Power
  - Short Circuit between Power and Ground during transition
  - Internal Capacitance within a Gate

Static Power
- Subthreshold Leakage
  \[ I_{\text{sub}} = I_0 (e^{-V_{\text{th}}/S} [1-e^{-qV_{\text{ds}}/kT}]) \text{ (at } V_{\text{gs}} = 0) \]
- Gate Leakage
90 nm Leakage vs Delay

- **loff (nA/µm)**
- **Gate Delay (ps)**

- **loffn**
- **loffp**
90nm Low $V_{th}$ & High $V_{th}$ Cells
Multi-$V_{th}$ Optimization Results
Case Study: 210K instances, 300MHz, initial leakage ~20uW

<table>
<thead>
<tr>
<th></th>
<th>Pre-route</th>
<th>Post-route</th>
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<tbody>
<tr>
<td></td>
<td>1-pass</td>
<td>Cell Swap</td>
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<tr>
<td>Physical Opt.</td>
<td></td>
<td></td>
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<tr>
<td>$Leakage\ (\mu W)$</td>
<td>10.8</td>
<td>11.1</td>
</tr>
<tr>
<td>$High-V_{th}\ (%)$</td>
<td>87.5%</td>
<td>89.7%</td>
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Meets timing – same slack as before Multi-$V_{th}$ Opt
Checks DRC for better design QoR and closure
Multi-Voltage Design Styles

Multiple Supply Multi-Voltage Islands
- Voltage areas with fixed, single voltages

Dynamic Voltage Scaling
- Voltage areas with fixed, multiple voltages
- Software controlled modes

Adaptive Voltage Scaling
- Voltage areas with variable $V_{dd}$
- Software controlled modes

IEM Partnership
Multi-$V_{DD}$ Design

- Isolation cells and level shifters for routing across voltage areas
  - Timing Constraints
  - Clock Frequency
  - Power
- Automatic insertion, optimization & power routing of special cells
  - Isolation cells
  - Level shifters
  - Retention registers
Power Gating

• Shut down non-active blocks
  ▪ Reduces leakage power
  ▪ Savings can be > 99%

• State Options:
  1) Throw away
  2) Scan out to memory
  3) Retain locally in “retention” registers

• States are restored or re-initialized when the blocks are reactivated

• Requires isolation cells at the boundaries
Leakage (Gated Ground or $V_{DD}$)

“Header”

Virtual $V_{DD}$

“Footer”

Virtual $V_{SS}$
Leakage (Gated Ground or $V_{DD}$)

1 Transistor / Cluster

Gate Transistor in Cell
Example Retention Register
Retention Register Insertion in Synthesis

- Same functionality, different styles
  - Additional restrictions on cell swapping
- Styles on HDL blocks
  - Set power gating style on named *always* blocks in Verilog or VHDL *processes*
- Control pins (save & restore)
  - Specially handled in synthesis
- Additional features supported
  - Scan Cells
  - Compile with gate level design
  - Incremental compile
  - Physopt
Power Compiler RTL Clock Gating
*Synchronous-load-enable Implementation*

```
always @(posedge CLK)
  if (EN)
    D_OUT = D_IN
```

Standard Non Clock Gating Implementation

Power Compiler Gated Clock Implementation
Challenge:
Concurrent Placement, Timing, Power & Clocking

- Power
  - Peak & Average
  - IR Drop
- Clocking
  - IR Drop
  - Max. Frequency
- Timing
  - Skew
  - IR Drop
- Placement
  - Skew
  - Path Delays & Slew
Synopsys Multi-Voltage Flow
Multi-Supply, Multi-Voltage Islands, Multi-Threshold Design

- Support throughout implementation & sign-off flow
- Multi-Voltage & Multi-Threshold synthesis in DC
- Power plan synthesis in JupiterXT
- Multi-Voltage placement & Multi-Threshold optimization in PC
- Multi-Voltage clock-tree synthesis & routing in Astro
- Sign-off with PrimeTime
AMBA DesignWare for AHB & APB Subsystems

- VDDRAM Domain
  - 16k Instruction RAM, 16k Data RAM
- VDDCPU Domain
  - ARM926EJ
    - 16k I-cache, 16k D-cache
- Dynamic Clock Generator
  - PLL1, PLL2
- Isolation Clamps
  - CPUCL (current), HPMCL (target)
- Level Shifters / Re-timing Interface
- Advanced High-Speed Bus
  - D-DW_AHB
  - I-DW_AHB
- Direct Memory Access
  - DW_DMA
- Interconnect Matrix
  - DW_ICM, x2
  - DW_ICM, x3
- Power, Clock, Reset, and Test
- Static Memory Controller
  - DW_Memcctl
- Dynamic Memory Controller
  - DW_Memcctl
- Digital Audio Controller
- SRAM, FLASH, CompactFlash x2 Interface
- SDRAM Interface
- IP Key:
  - ARM - light blue
  - National - dark blue
  - Artisan - yellow
  - Synopsys - purple

- Multi In-Circuit Emulator Sync
  - Advanced Power Controller Interface
  - Real-Time Clock DW_RTC
  - Interrupt Controller DW_IntrCont
  - Timers x2 DW_Timers
  - General Purpose I/O x48 DW_GPIO
  - Universal Async Receiver/Transmitter DW_UART_0
  - Universal Async Receiver/Transmitter DW_UART_1
  - Serial Synchronous Interface DW_SSI
Synopsys supplies:

- Low Power IEM Design Methodology
- Multi-voltage Galaxy Implementation Flow
- AMBA DesignWare IP
- Low Power Design Services