Way Beyond Waveforms

Interoperability With SystemVerilog

SystemVerilog

Novas
Mission:
Automate and simplify the design comprehension and debug process, allowing engineers to productively focus on problem solutions

- **#1 Customer satisfaction**
  - 2002 EETimes EDA user survey
- **#1 Market share**
  - 2002 Gartner/Dataquest EDA market report
- **10,000 seats in use at 400+ companies**
- **35+ EDA / IP partners using Novas technology**
- **Technology Excellence**
  - 225 people, 100+ engineers
  - Focus on
    - Debug automation
    - Design comprehension
    - Methodology coverage
- 50% verification resource on debug, 70% project resource on verification
- Cost per US engineer approximately $150K, cost of debug 35% of this
- Therefore, debug costs $53K per US engineer per year, takes 1/3 of their time

Source: Novas Customer Survey, 161 Respondents
Comprehensive Debug Requires More Than Simple Visualization
Automating Debug
Critical Productivity Enhancement

Utilizing behavior based debug to automate time consuming aspects of debug process

- Time and structure in single view
  - Immediate visual of design behavior
- Automated cause / affect tracing
  - Understand problem areas quickly
- Link back to regular views
  - Bind problem to modeling issue

EDN Magazine Innovation Award 2002 Finalist

Novas Software, Inc. • Way Beyond Waveforms
Novas Unified Interoperability
Key For SystemVerilog Inclusion

Design & Verification Process

- Specification
- Block
- Chip

Tools

Languages

Unification:
Same Ideal As SystemVerilog

- Open architecture
  - extensibility for future processes
- Eases learning curve, makes usage, tool chain more efficient
- Single Novas environment covers range of tools and languages
  - 38+ Partner tools using Novas technology as viewers
  - Covering major design, testbench, systems and assertion languages
- SystemVerilog 3.0 capabilities
  - New Verilog constructs and keywords recognized
  - Structures, types, etc. available, similar to VHDL
  - SV ‘Interface’ debugging also available
Debugging SystemVerilog Assertions

- Wide range of assertion languages
  - PSL, OVA, OVL – forerunners to SV
  - SystemVerilog

- Powerful assertion debug
  - View assertion / design association
  - Check new assertions without re-simulation
  - Assertions can drive debug process

Novas Software, Inc. • Way Beyond Waveforms
SystemVerilog 3.1 Testbench

- Testbench capabilities expected
  - Testbench features, OO, coverage, etc available
  - SystemVerilog testbench-design unification carried through to unified debug system
  - Similar to Vera debug

---

SV 3.0 Beta | SV 3.0 Prod. | SV Assertion Beta | SV Assertion Prod | SV 3.1 Testbench

Novas Software, Inc. • Way Beyond Waveforms
Multi-lingual Methodology Extension

- Wide range of languages covered
  - **SystemVerilog** general purpose
  - **Vera** / 'e’ testbench
  - **PSL, OVA, OVL** assertions
  - **SystemC** system modeling

- Powerful assertion & testbench debug
  - View assertion / design association
  - Drive debug process using assertions
  - One environment for design & testbench

- System Platform Debug
  - Monitor range of platform components

Verification Environment Debug

- Automated Test
- **Assertions VIP**
- **Results Analysis**
- **DUT**
- **Functional Coverage**

System Platform Debug

- **Transaction debug**
- **Testbench / assertions**
- **HW/SW**
- **Understanding IP**
- **Protocol debug**

Novas Software, Inc. • Way Beyond Waveforms
Broad Partner Base
Utilizing Novas Technology

- 0-In
- Aldec
- Antrim
- Averant
- Avery
- Axis
- Cadence
  - Quickturn
  - Silicon Perspective
  - Verplex
- Celestry
- CoWare
- Denali
- EverCAD
- Fintronic
- Forte
- HD Lab (Japan)

- Incentia
- Jasper
- Legend
- Manhattan Routing
- Mentor
  - IKOS
  - Model Technology
- Nassda
- Real Intent
- Simpod
- Synopsys
  - InnoLogic
  - Co-Design
- SynTest
- Tharas
- TransEDA
- Valiosys
- Verisity
Novas Software, Inc.  •  Way Beyond Waveforms

- Debug is a major productivity bottleneck
  - 50% of engineering intensive time

- Advanced debug technology dramatically improves engineering efficiency
  - Automation, Comprehension, Unification

- Novas is undisputed technology and market leader
  - SystemVerilog execution against plan example of this