Next-Generation Analog-Mixed Signal & Custom Digital EDA

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Founder of SDA / Cadence
Over $700M Analog-MS & Custom EDA Market

$ in Millions*

1 Analog/RF Simulation
2 Fast Digital Spice
3 Custom Layout
4 Parasitic Extraction
5 Design Entry
6 Interactive DRC, LVS, ..
7 Synthesis (Elect & Phys)
8 M-S Verification
Behavioral Sim
Automated Analog Layout
Next Gen Design Environment (future)

* Sources: Designers Guide Consulting, EDAC, DataQuest
Designer’s Needs are Changing

- About 80% of all SOC design starts are now mixed-signal*
  - Cell phones, wireless LAN’s, GPS’s, MP3 players, PDA’s, HDTV’s, …
- This is causing major changes in design methods
  - Today’s tool flows are breaking
- EDA suppliers without analog have incomplete solutions
  - Even Cadence is weak in mixed-signal
- Custom digital is similar - too little automation
  - Sub-100nm nodes force analysis at transistor & wire level

*Estimates from Designer’s-Guide Consulting
Mixed-Signal SOC’s that Break Today’s Design Flows

Some Examples
Algorithmic Mixed-Signal Radio* for Cell Phones, other

* Texas Instruments & others
Algorithmic Radios

How do we design these?

• Problem:
  – Cannot simulate the analog-digital loop today - too big
• Should use fast Harmonic Balance for RF, but:
  – Must use time domain to handle gates + analog: Spectre or HSpice
• Spectre & HSpice are much too slow for 150k transistors
• Need new a transistor-level simulator:
  – Fast analog Spice that has ~100x speedup at full Spice accuracy
802.11G Wireless LAN Chip*

- New process nodes give:
  - Poor analog transistors, cheap gates
- Use digital correction to fix analog
  - DC offset, I/Q mismatch, RF leakage
- Analysis requires transistor-level simulator
  - Handle ~100k transistors, 10k cycles

* 2005 ISSCC Paper 5.2 Atheros, Stanford
Multi-channel Digital-Audio Amp*

Need to verify chip & test power “modes”, & speaker pop

* D2Audio design
Multi-channel Digital-Audio Amp

*How do we verify this 10M gate design?*

- Today’s FastMOS simulators (HSIM, etc) not good enough
  - In analog mode: little speed-up over Spice, may not converge
- Requires a next generation FastMOS simulator
  - Must handle 10M transistor random logic + memory, some analog
  - Need ~10,000x speed-up over Spice, robust convergence on analog
Wideband Blocks for HD TV
RF & Wideband Amps, ADCs, PLLs, Oscillators

Design for low distortion, high precision

RF video amps, baseband amps
Broadband Blocks for HD TV

*How do we design these?*

- **Typical today**
  - Layout is manual, cannot extract parasitics until design done
  - Use rough guesses at parasitics during design – *accuracy poor*

- **Big issue**: Need early simulation with accurate parasitics

- **What is needed:**
  - Analog-constrained floor planner, placer, router – “automated” & quick
  - Tightly coupled layout & schematics for rapid incremental change & re-simulation - [OpenAccess db](#) is designed for this
What about Reusable Analog IP?

- Need powerful expression handler
  - Captures all electrical & physical design equations
  - When IP is reused, have all info needed to retarget block
- Need standard design kits – electrical & physical
  - Technology, symbols, transistor models, ... OK initiative
  - Physical layout based on PyCells* so can retarget design & process
- Need a OPEN user extension languages: Python, Tcl
  - Python: Rich, open, portable, no pointers, 10x productivity over C++
  - Lets user customize design flows & write simple tools

* Python language-based pCells = PyCells
A Next Gen Analog Mixed-Signal Design System

Most of needed capabilities identified by our design examples
Next Gen Analog-MS Design System

- **Schematic Editor & Cockpit**
- **Matlab-Based System Simulator**
- **Expression Handler**
- **Waveform Display**
- **Extension Languages**
- **Test Benches**
- **Circuit Synthesis**
- **Verilog-A/VHDL-A**
- **Automated Analog P&R**
- **Custom Layout**
- **Optimizer**
- **Fast A/M-S/RF SPICE**
- **Python PyCells**
- **Incremental DRC**
- **RLC Extraction**
- **FastMOS Digital SPICE**
- **OpenAccess database**
- **Harmonic Balance**
- **EM Simulation**

- = **New tool needed**
- = **Existing tool**
- = **Highest impact**
Major Features of a Next Gen Analog Design System

• Design creation using schematics and language
  – Every component described by a design equation
  – Captures all design knowledge for IP export & reuse

• Incremental design
  – No netlisting - rapid read-in & quick changes, huge circuits

• Automatic tracking of dependencies
  – Change a device parameter & auto-ripples though system
  – Today’s manual system has numerous points of failure

• Assertion-based design
  – Set design limits - if violated, simulator stops, gives feedback
Major Features of a Next Gen Analog Design System (cont.)

- Early post-layout simulation with parasitics
- PDK automation, both electrical & physical
- Co-design with groups in remote sites
- Large project task management
  - Auto-launch multiple simulations into compute farms
  - All aspects of design results archived & accessible
- Single unified user cockpit – simulation control, analysis, optimize, results
  - All tools accessible from single screen, prevents user errors
- Native on OpenAccess
Do We Really Need a Next Gen System?

- FW’s, db’s & tools need to be re-written every 7-10 yrs
  - Design styles, processes & target markets change
  - The Analog Artist/Virtuoso system completed in 1990, 15 years ago!
- Many flows kludged together from acquisitions
  - db translations, slow, error prone, poor usability, inflexible
- Much of today’s code base is old, needs re-write
  - Companies keep evolving old code, quality worsens
- Cost of maintaining legacy code is huge
Summary: Next Gen Analog

- Existing Analog EDA Systems are aging badly
  - Users have critical new needs: RF, mixed-signal, & fast digital SOC’s
- Significant new tools & environments can dramatically help
  - Analog-constrained automated layout
  - Ultra fast transistor-level simulators – analog & digital
  - Open extension languages (Python, Tcl ...) enable portable IP
  - New design environment - incremental design, ...
- New capabilities in OpenAccess enable next gen capabilities
- Startups & EDA leaders making good progress with all this
END